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Performance evaluation of enhanced pulse width modulation techniques for cascaded multilevel inverter

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ABSTRACT

The nine-level multi-level inverter (MLI) uses a DC voltage supply, seven switches, four capacitors, and twelve diodes to generate an AC output with nine distinct voltage levels. Control strategies like pulse width modulation (PWM), fuzzy logic control (FLC), and time ratio control (TRC) regulate the inverter's performance. Multi-carrier PWM techniques such as APOD, POD, PD, and multi-reference PWM are applied for precise control. The system is simulated in MATLAB, and performance is evaluated based on output voltage RMS and total harmonic distortion (THD), ensuring compliance with IEEE standards. FLC and TRC have been proposed as control approaches for the mighty nine-level MLI. The proposed inverter uses 60% fewer components than traditional designs while giving better power quality. All methods performed better than existing field-programmable gate array (FPGA)-based systems that had 19.86% THD. The performance evaluation includes output voltage rms and THD indices, requirements that must meet IEEE standards. The proposed strategies are compared with existing techniques in the literature.

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1. INTRODUCTION

In the last decade, researchers have developed a variety of multilayer inverter topologies. Regular inverters create poor quality of electricity with lots of harmonics. This causes problems in electrical systems. Multi-level inverters (MLIs) are better but use too many switches and are expensive. Control signals for the multilayer inverter are often generated using traditional control techniques. For the control of MLI, artificial intelligence, neural networks, genetic algorithms, and other methods are being developed. Three control strategies for the nine-level MLI are proposed in this study. Pulse width modulation (PWM) control, fuzzy logic control (FLC), and time ratio control (TRC) are the three methods. This chapter discusses the three proposed control techniques. A new nine-level MLI has been designed. The proposed control strategies are tested on the performance of a simplified H-bridge nine-level inverter. The proposed control approaches and the simplified nine-level MLI are developed using MATLAB. To assess their performance, various types of loads are evaluated. Each regulatory strategy's effectiveness is assessed using the generation of total harmonic distortion (THD). As the number of layers rises, the output voltage waveform of a multilayer inverter tends to become more sinusoidal [1], [2].

The proposed power arrangement employs the fewest possible switches. It has seven switches for the MLI's nine levels. Because managing seven switches is simple, a nine-level MLI is being explored [3]-

[5]. Inverters must be able to handle high voltage and high power in applications like those listed above. The uneven distribution of the applied system voltage through the devices, which can cause the applied voltage of individual devices to be significantly higher than the device's blocking voltage during the transient and steady state switching operations of the devices, is a significant problem with the serial connection of switching power devices [6]-[9]. To successfully address the issues above, various multilayer inverter and converter circuit topologies have been investigated and employed as alternatives. The MLI's output voltage has several levels synthesized from many DC voltage sources. The efficiency of the output voltage increases with the number of voltage levels, allowing for a reduction in the number of output filters [10]-[16]. In multi-level systems, precise commutation is necessary due to circuit complexity and many power switches. It recommended an inverter topology to address these two problems. To significantly minimize the complexity of the power circuit, this architecture combines an H-bridge stage with an auxiliary bidirectional switch. It streamlines the implementation of modulator circuit design by using a modulator firing control circuit built using a field-programmable gate array (FPGA) programmable circuit [17]-[25].

2. SUGGESTED TOPOLOGY OF MULTI-LEVELINVERTER

The compact nine-level inverter has one DC supply, seven switches (S1-S7), our capacitors, and twelve diodes. The four capacitors each receive an equal amount of the incoming DC voltage. There are as few components as feasible in this nine-level MLI. Four switches are used to create the H-bridge. Using switches S1 and S4, positive voltage is provided across the load. Using switches S2 and S3, the negative voltage is applied across the load. Switches S5 through S7 provide a range of voltage values. Switch S5 is used to link diodes D1 through D4, switch S6 is used to connect diodes D5 through D8, and switch S7 is used to connect diodes D9 through D12. Blocks for measuring voltage and current have been added. The circuit has a scope that shows the voltage and current. The 9-level MLI has been condensed using MATLAB. A sub-system of the suggested time ratio regulating technique is also created in MATLAB.

A single-phase inverter is typically used for applications requiring less than one KW. A multilayer inverter's output voltage waveform consists of voltages collected from numerous tiny DC voltage sources. On the other hand, the proposed nine-level inverter structure only requires one DC voltage source. The new inverter topology used in the power stage is considerably improved regarding component count and layout complexity. The new topology for nine-level inverters employs fewer diodes and capacitors and requires over 60% fewer main power switches than conventional topologies. From a five-level inverter, the single-phase nine-level H-bridge inverter was created. The four major power devices, S1 to S4, make up the H-bridge. C1, C2, C3, and C4 make up a capacitor voltage divider. Figure 1 shows the auxiliary switches, which comprise the controlled switch and four diodes for each switch.

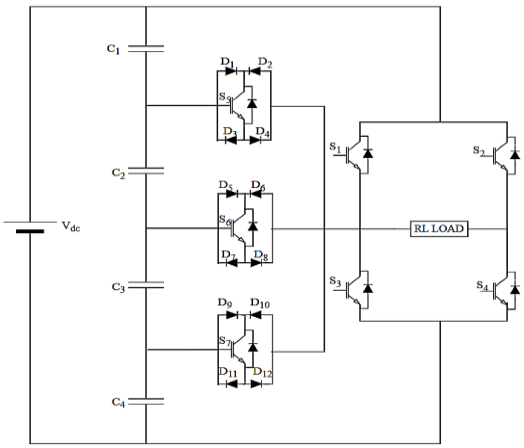

Figure 1. Proposed topology of nine level MLI

The compact nine-level inverter has one DC supply, seven switches (S1-S7), four capacitors, and twelve diodes. The four capacitors each receive an equal amount of the incoming DC voltage. There are as few components as feasible in this nine-level MLI. Four switches are used to create the H-bridge. Using switches S1 and S4, positive voltage is provided across the load. Using switches S2 and S3, the negative voltage is applied across the load. Switches S5 through S7 provide a range of voltage values. Switch S5 is used to link diodes D1 through D4, switch S6 is used to connect diodes D5 through D8, and switch S7 is used

to connect diodes D9 through D12. Blocks for measuring voltage and current have been added. The circuit has a scope that shows the voltage and current. The 9-level MLI has been condensed using MATLAB. A sub-system of the suggested time ratio regulating technique is also created in MATLAB. Figure 2 displays the nine-level MLI's TRC and streamlined version.

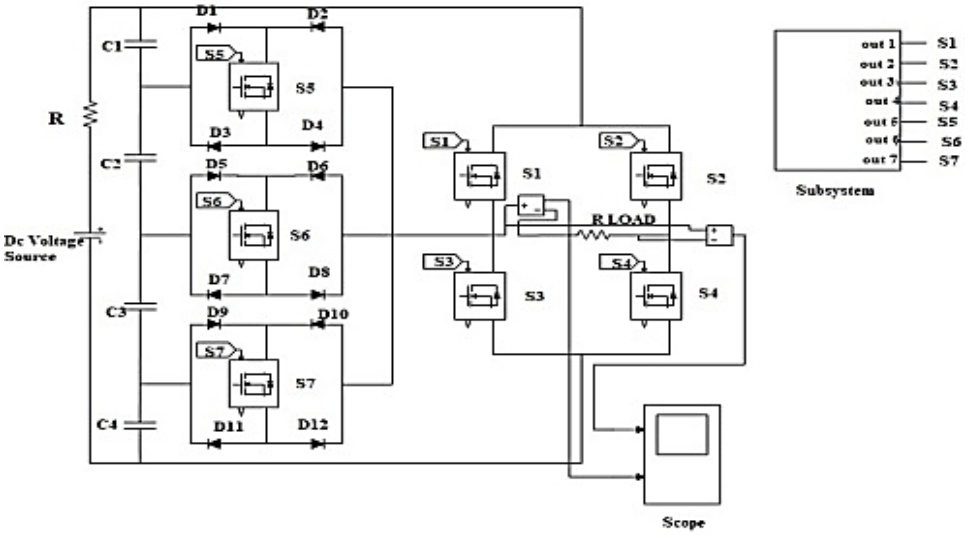

Figure 2. Simplified H-bridge 9-level inverter

For R-type loads, the effectiveness of the TRC strategy is assessed. 101 Ω and 51 mH, respectively, are the values for R and L. Control signals are created via constant frequency control. The period is kept constant while the ON time varies in the constant frequency control. The period is set to 0.021 sec to obtain a frequency of 50 Hz. Control signals are produced using multiple pulse generators. Figure 3 displays the control signals.

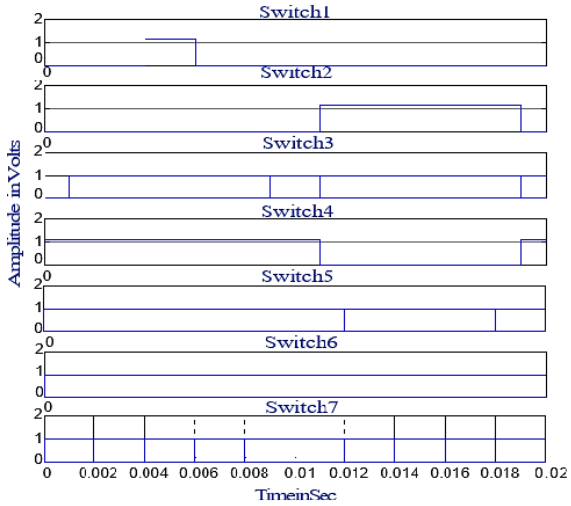

Figure 3. Switching pulses for switches S1 to S7 in TRC controlling technique

The output voltage of the nine-level MLI, which has been streamlined for an R-type load, is shown in Figure 4. 114 volts DC is the input voltage. The output voltage is available in nine levels. The nine levels of the output voltage are 0 V, 28.76 V, 114 V, 86.23 V, 57.52 V, 57.6 V, and 86.23 V. The output voltage's rms value is 106.81 V. Figure 5 displays the output current. The output current waveform is sinusoidal in shape. The output current is 0.23 A in value. Figure 6 displays the overall harmonic distortion. 1.631 harmonics are distorted in total.

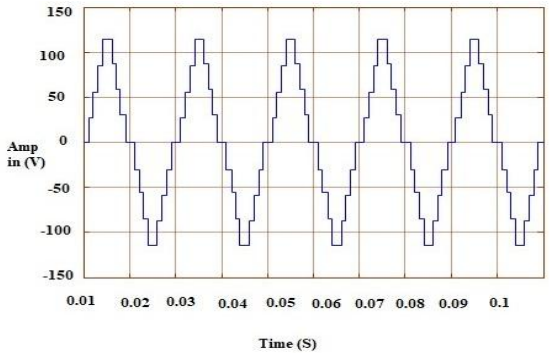

Figure 4. Output voltage of 9-level MLI with R load (TRC)

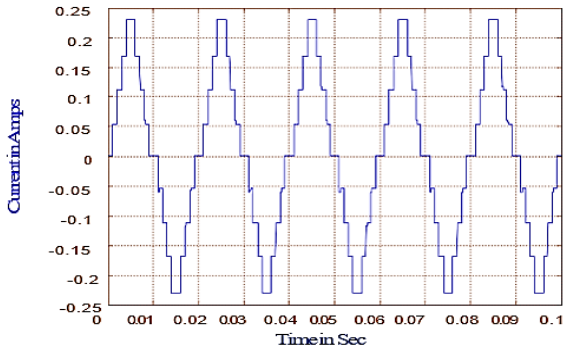

Figure 5. Current in 9-level MLI with R load (TRC)

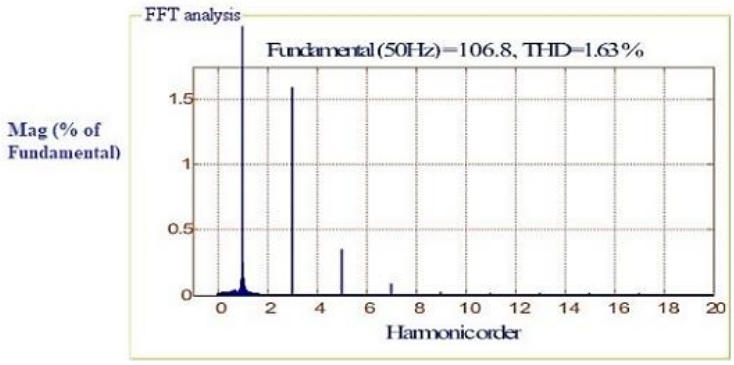

Figure 6. THD of 9-level MLI with R load (TRC)

3. RESULS AND DISCUSSION

3.1. Performance of APOD MCPWM controlling technique

In this alternate phase opposition disposition multi-carrier PWM controlling approach, eight triangular carrier signals-half positive and half negative-plus one sinusoidal reference signal are creatively combined to generate seven control signals for the condensed nine-level MLI. Vr(1) to Vr(8) represent each of the magnitudes of the respective triangle carriers, while Vs denotes that of the sinusoidal signal, as depicted. This sub-system truly puts a unique twist on traditional PWM regulating. An R-type load with R equal to 100.1 is used to test the alternate phase opposition disposition multi-carrier PWM controlling approach.

Figure 7 displays the MLI's output voltage. The output voltage has nine stages and a rms value of 112.81 V. Figure 8 displays the MLI's output current. The output current waveform resembles a sinusoidal wave more closely. The entire harmonic distortion is shown in Figure 9.

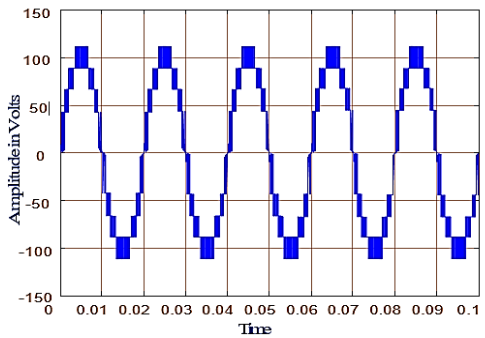

Figure 7. Output voltage of H-bridge 9-level MLI with R load (APOD)

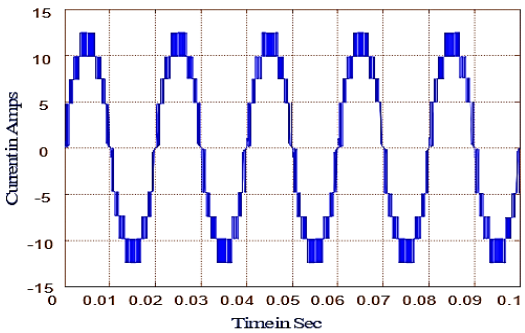

Figure 8. Output current of H-bridge 9-level MLI with R load (APOD)

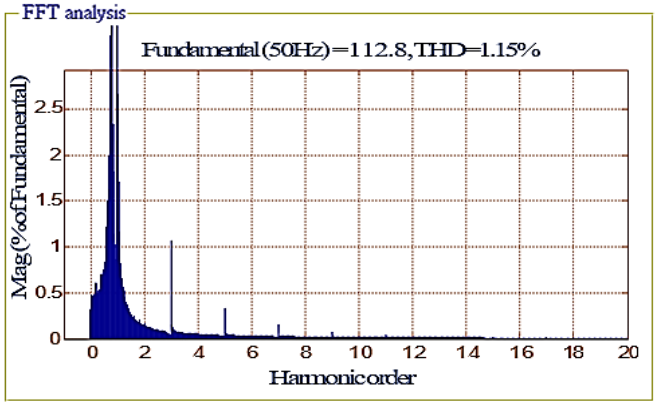

Figure 9. THD of H-bridge 9-level MLI with R load (APOD)

3.2. Performance of PD MCPWM controlling technique

This phase opposition disposition multi-carrier PWM control technique utilizes a single sinusoidal reference signal to generate seven control signals for the proposed nine-level MLI. The method employs four positive and four negative triangular carrier signals with matched phase characteristics, and the control signals are generated by applying compacted triangular amplitudes Vr(1) to Vr(8) along with a sinusoidal reference Vs of equal magnitude. The proposed phase disposition multi-carrier PWM regulating strategy is evaluated for an R-type load where R=100.1 Ω. Figure 10 displays the MLI's output voltage. The output voltage has nine levels and a rms value of 107.51 V. Figure 11 displays the MLI's output current. The output current waveform resembles a sinusoidal wave more closely. Figure 12 displays the overall harmonic distortion. THD is measured at 1.212.

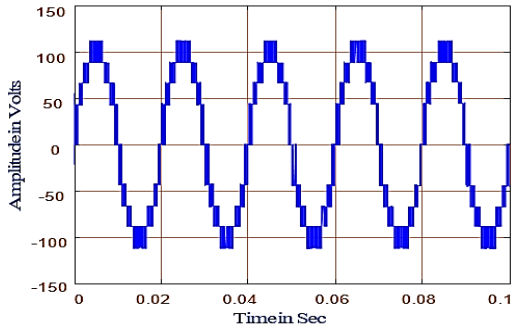

Figure 10. Output voltage of H-bridge 9-level MLI with R load (PD)

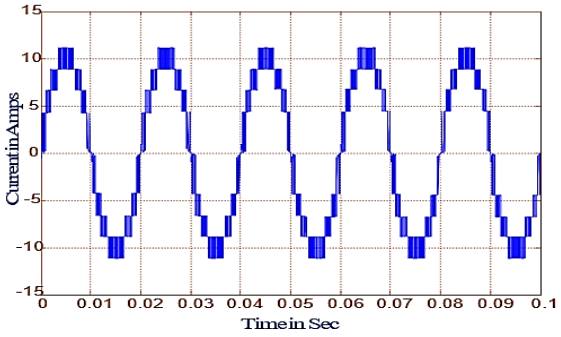

Figure 11. Output current of H-bridge 9-level MLI with R load (PD)

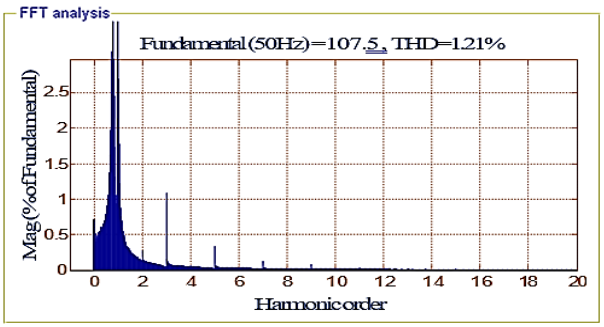

Figure 12. THD of H-bridge 9-level MLI with R load (PD)

3.3. Performance of multi-reference pulse width modulation controlling technique

Eight sinusoidal reference signals and one triangular carrier signal are used in the multi reference PWM controlling approach. Four sinusoidal impulses are in phase, while the others are 180 degrees out of phase. The procedure generates seven control signals for the condensed nine-level MLI from the eight reference sinusoidal signals and one triangular carrier signal. Vs(1) to Vs(8) represent the magnitude of reference signals, and Vr denotes the magnitude of triangular signals. The multi reference PWM regulating method is evaluated with an R-type load of 100.2 Ω. Figure 13 displays the MLI's output voltage. With nine levels, the output voltage has a rms value of 114.81 V. Figure 14 depicts MLI's output current. The output current waveform resembles a sinusoidal wave more closely. In Figure 15, the overall harmonic distortion is displayed. THD is measured at 1.41.

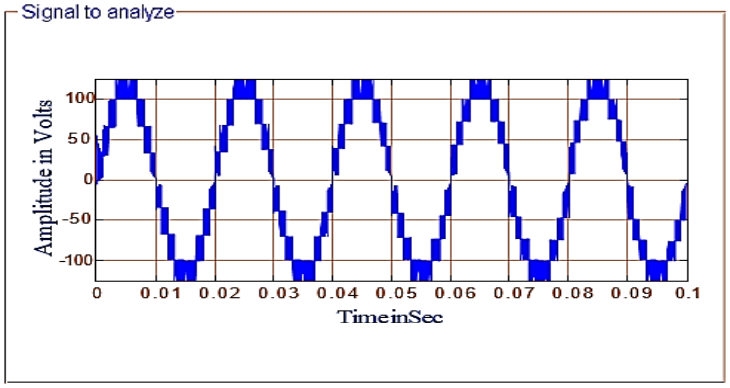

Figure 13. Output voltage of H-bridge 9-level MLI with R load (MRPWM)

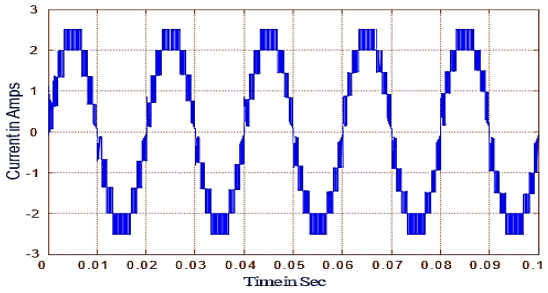

Figure 14. Output current of H-bridge 9-level MLI with R load (MRPWM)

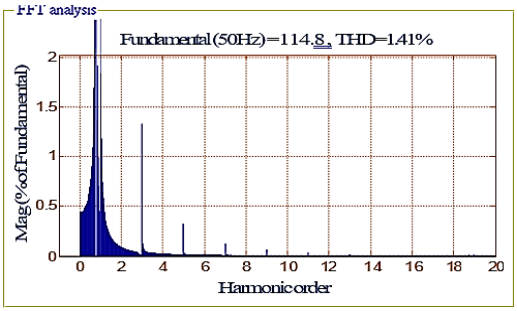

Figure 15. THD of H-bridge nine-level MLI with R load (MRPWM)

3.4. Performance of fuzzy logic control technique

An intelligence technology called FLC solves various electrical issues. FLC can be used whenever a suitable mathematical model is unavailable. Based on the system's knowledge base, solutions can be found. Using the skills and information described above, a very effective fuzzy logic system can be created. Researchers have developed numerous FLC systems for power electronic converters and inverters. FLC needs two inputs: the error and the change in error in the output voltage of the nine-level MLI. The output sends a control signal to the multilayer inverter. The control signal (duty cycle) is combined with PWM to produce control signals for each switch in the multilayer inverter. When R is 100.1 Ω, the FLC regulating method is tested for R-type loads.

Figure 16 displays the MLI's output voltage. With nine levels, the output voltage has a rms value of 113.1 V. Figure 17 depicts MLI's output current. The output current waveform resembles a sinusoidal wave more closely. In Figure 18, the overall harmonic distortion is displayed. THD has a value of 0.75.

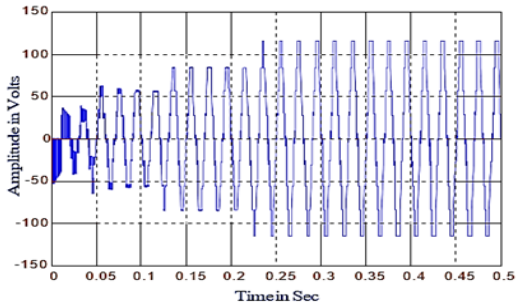

Figure 16. Output voltage of H-bridge 9-level MLI with R load (FLC)

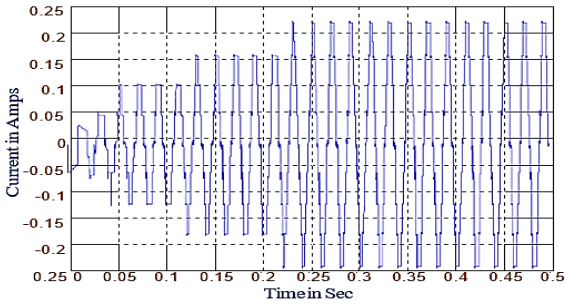

Figure 17. Output current of H-bridge 9-level MLI with R load (FLC)

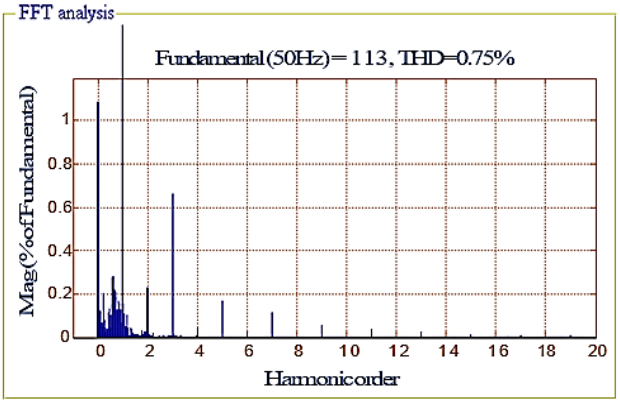

Figure 18. THD of H-bridge 9-level MLI with R load (FLC)

3.5. Comparative analysis of various pulse width modulation strategies

The recommended control techniques are compared. The multi-reference PWM technique produces a larger output voltage than other methods. The nine-level simplified MLI output voltage has reduced THD thanks to the fuzzy logic regulating technology. The TRC regulating technique produces more harmonics than other suggested ways. Table 1 compares the nine-level MLI's output voltage and THD to those of other methods. According to Table 1, the proposed control strategies outperform the MLI with FPGA control in terms of THD. Table 2 shows comparative analysis of THD. The above control methods produce THD more effectively than the IEEE standard.

Table 1. Comparative analysis of THD and TR for different methods with PBBO-FOPID

Control techniques	R load	
	Output voltage (volts) (rms)	% THD
TRC	106.81	1.631
APOD MCPWM	112.81	1.151
POD MCPWM	110.81	1.171
PD MCPWM	107.51	1.212
MRPWM	114.81	1.41
FLC	113.1	0.75
FPGA control based MLI	25.25	19.86
IEEE standard	---	5

Table 2. Comparative analysis of THD

Topology	Switch count	Control method	THD (%)	Source type
Cascaded H-bridge (CHB)	16	SPWM	~12	Multiple DC
Diode-clamped (NPC)	18	SVM	~10	Single DC
Flying capacitor (FCMLI)	20+	Carrier-based PWM	~9	Multiple DC
Hybrid MLI (Pandey *et al.* [25])	12	Embedded PWM	~8.5	Mixed sources
Proposed MLI (this work)	7	FLC, TRC, and PWM	<6.5	Single DC

4. CONCLUSION

This paper presents a groundbreaking design that requires only seven switches, twelve diodes, four capacitors, and one DC source, exploring the possibilities of a nine-level MLI. Utilizing an H-bridge to alter the supply's polarity to the load with four switches and three additional switches adding four further voltage levels, resulting in a total of nine output voltage levels. With its application of MATLAB in constructing and testing TRC, PWM, and FLC strategies implemented through multi-carrier PWM techniques such as alternate phase opposition disposition, phase opposition disposition, multi-reference, and phase disposition, this machine shows excellent performance in THD reduction. Showcasing these impressive capabilities is especially effective under fuzzy logic parameters, while TRCs seem most efficient in creating harmonics. Combine control methods (like FLC with TRC or VSG) to get better performance in weak or unstable grids.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Jayaprakasam Vinothini	✓	✓	✓		✓				✓	✓				
Ravindran Ramkumar	✓				✓	✓				✓	✓	✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

INFORMED CONSENT

We have obtained informed consent from all individuals included in this study.

ETHICAL APPROVAL

The research related to human use has been complied with all the relevant national regulations and institutional policies in accordance with the tenets of the Helsinki Declaration and has been approved by the authors' institutional review board or equivalent committee.

DATA AVAILABILITY

The data are available from the corresponding author upon request.

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