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Design and development of photovoltaic solar system based single phase seven level inverter

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ABSTRACT

For solar photovoltaic (PV) systems, an upgraded triple gain seven-level inverter that works both independently and while connected to the grid is proposed. The two-stage configuration of the system is boost cascaded. The first stage has a one switch improved gain converter (OSIGC) to increase and normalize the input direct current (DC) voltage, and the second stage includes a unique seven level alternating current (AC) is produced via a multilevel inverter (MLI) design with triple voltage gain. The proposed OSIGC is appropriate for a broad range of conversions. The voltage gain in MLI was achieved using switched capacitor techniques. The DC-DC converter can achieve a maximum voltage gain of twelve and the MLI can achieve a maximum voltage gain of three, resulting in a DC-DC-AC voltage that can reach 36. Maximum power point tracking (MPPT) technique based on modified perturb and observe (P&O) is used in OSIGC to maximise PV module power utilisation, and MLI control utilises sinusoidal pulse width modulation (SPWM) realistically. For the purpose of analysing the suggested system, a 200 Watt prototype statel is created. With a total harmonic distortion (THD) of 0.181%, up to 92.12% of the converter system's overall efficiency is possible.

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1. INTRODUCTION

Energy use increased as a result of extensive industrialization and population growth. By simulating global warming, the usage of traditional energy sources boosted carbon dioxide emissions and led to adverse problems. To substitute for traditional energy sources, researchers are working nonstop to create alternative energy sources. Alternative energy is beneficial replacement for traditional ones. Contrary to popular belief, unconventional energy sources are expensive to develop and have low efficiency. It is common practise to obtain electrical power from unconventional sources using fuel cells, small wind turbines, solar photovoltaic (PV) modules, and other technologies. To provide power to associated voltage sources that are cascaded, the majority of unconventional energy systems, which typically output unregulated low direct current (DC) voltages 12 V to 48 V, to controlled higher DC voltage levels (VSI), which they are designed to do. The converters used in the systems must possess a number of key characteristics, including low price, compact size, excellent efficiency and a wide conversion voltage range. Three types of DC-DC power converters are available: non-isolated, partially isolated, and isolated [1]–[5]. Over isolated bidirectional half-bridge and

full-bridge pulse width modulation (PWM) converters, partially isolated converters are favoured. Because isolated bidirectional half-bridge and full-bridge PWM converters are available, isolated converters (PIC) are a good option for a number of input and output ports. Low component counts help to avoid complex circuits, which is a major feature of partially isolated converters.

In contrast, voltage regulation was not very good in partially isolated converters, which limited the effects of applications requiring high voltage stress and minimal power. Additionally, there are serious consequences when a single component fails. When galvanic isolation is not required, non-isolated converters are employed in a wide range of conversion applications. The load has been spread out thanks to semiconductors and reactive components. For high voltage conversion, an inductor connected to the converter is recommended in the converters mentioned in [6]. With a 1:1 transformation radio, ferrite cores are used to create coupled inductors. Coupled inductor-based converters have significant electromagnetic interference (EMI) problems, making them unsuitable for high-frequency operation. For a high conversion ratio, voltage doubler circuits [7] are employed, along with two additional reactive components. The voltage doubler circuits benefit from operating at a high frequency. High power applications are preferred for interleaved converters [8], [9]. Since they need for more inductors, switches, linked inductors, and transformers. The static gain is reduced when switches are engaged during a different period, making control difficult. Cascaded boost converters, which are two basic boost converters connected in series to provide a wide conversion range, are what [10]–[12] is referring to higher voltage gain was attained.

On the other hand, as there were more components and steps, the efficiency decreased. Snubbed circuits and complex control methods are necessary to lower noise and improve the performance of the cascaded converter. The single-ended primary-inductor converter (SEPIC), the Cuk converter, and the interleaved flyback converter are also choices for wide conversion ranges [13]–[19]. For low or high-duty radio operation, the aforementioned topologies lead to expensive and challenging driving circuits. Wide range conversion brought on by high voltage stress and parasitic resistances in the filter inductor results in significant losses, which negatively affect performance and lead to inefficient operation. To serve alternating current (AC) loads, commercial PV systems need to convert DC to AC. The obvious choice for a smooth functioning is a multilevel inverter [20]–[22]. Multilevel inverter (MLI) is regarded as meeting the set AC output voltage and frequency requirements, decreased total harmonic distortion (THD), and voltage fluctuation restrictions. It was crucial to create a converter with good voltage conversion and minimal voltage stress across switches as a result of the considerable research. The easiest technique to get a high voltage conversion ratio and little switching voltage stress is to incorporate a voltage multiplier circuit into the boost converter circuit already in place. The input voltage is frequently raised using DC-DC converters, and high voltage DC to AC is subsequently converted using DC-AC converters. The performance of the power systems as a whole should be significantly impacted by the choice of the DC-DC converter [23]–[30].

2. ANALYSIS OF ONE SWITCH IMPROVED GAIN CONVERTER

The structure of the one switch improved gain converter (OSIGC) is shown in Figure 1. While the photovoltaic unit is linked to the DC input port as low voltage, the multilevel inverter is attached to the enhanced voltage output port. The PV module's output power is determined by how much light strikes it, and its output voltage varies with light intensity. A Luo super lift circuit is created by the inductor L1 and capacitor C1. Inductor L2 is merged to accomplish a broad conversion range, use the Luo super lift circuit. An inductor L1, L2, and C1 link the diodes D1, D2, and D3. The output DC port of the MLI is connected to the filter capacitor (CF), which aids in maintaining a steady voltage throughout operation. Figures 2(a) and (b) depict Social Sciences and Humanities Research Council (SSHRC's) operational states. To lessen reverse current flow, D4 is wired between the output port and the high gain circuit. The PV voltage causes the diodes D1, D2, and D3 to be forward biassed at the time the switch "S" begins to conduct at time $t1$. PV current first enters the L1, L2, and C1. Diodes D1, D2, and D3 connect L1, L2, and C1 in parallel to the PV module. Solar energy is being harnessed to charge L1, L2, and C1. The PV's internal current (IPV) is equal to the total of the currents flowing through the capacitor C1, inductors L1, and L2. Due to the reverse bias of diode D4, the load is disconnected from the high gain circuit. The state-I capacitor's CF is in charge of supplying load power. Up until inductors L1, L2, and capacitor C1 are fully charged, switch S is turned on. When $t2$ arrives, state-I stops and state-II starts. Due to L1 and L2's degradation current, which occurs when state switch "S" is off, their polarity is reversed, which causes D1, D2, and D3 to be reverse biassed. The output port, PV, and forward-biased diode D4 are linked in series via C1, L1, and L2. There is a discharge of the L1, L2, and C1. Input voltages VPV, VL1, VL2, and VC1 are added together to provide the voltage (V0 (DC)) across the output port. The filtering capacitor (CF) capacitor is charging. At $t3$, the state-II comes to an end.

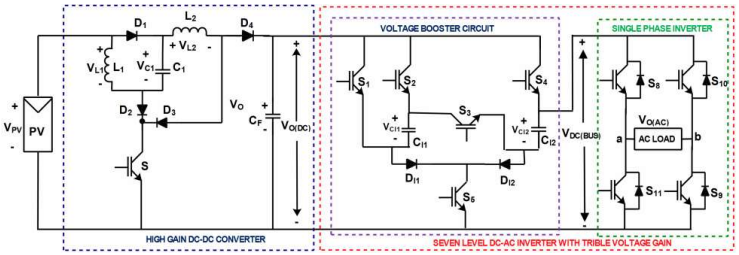


Figure 1. Planned converter DC to DC to AC

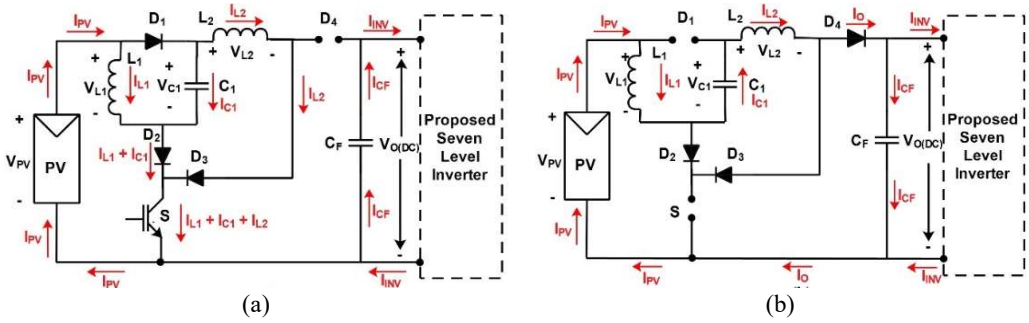


Figure 2. State of process of converter OSIGC: (a) state-I (on) and (b) state-II (off)

3. TRIPLE VOLTAGE GAIN SEVEN-LEVEL INVERTER

According to Figure 3, the MLI is built with an inverting circuit and a voltage booster. The MLI and OSIGC are linked in series. To carry out boost operations, the capacitors CI1 and CI2 are used. To achieve triple voltage gain, the capacitors CI1 and CI2 are regularly charged with OSIGC output power and drained through the load. With the aid of capacitors CI1 and CI2, the OSIGC output voltage (VDCbus) is increased to 2 V_{ODC} and 3 V_{ODC}. The MLI is built using five insulated gate bipolar transistor (IGBT) switches (S1 to S5), which connect the capacitors CI1 and CI2 with the OSIGC output and load. There are four operating states for voltage booster circuits, and each state enhances the output voltage of an OSIGC by a different amount of voltage. Each state's circuit state l is displayed in Figures 3(a) to (d).

State-I: Figure 3(a) depicts the analogous circuit state l for state-I. The inverting circuit is off, the switches S2, S4, and S5 are receiving pulses, while the remaining switches are in voltage boosting. The forward bias of DI1 and DI2 allows current from the OSIGC to travel to capacitors CI1 and CI2. Connected across the OSIGC output, the capacitors CI1 and CI2 are separately charged. The current from the capacitors is passing through the switches S2, DI1, S5, and S4, DI2, and S5. The capacitors' state of charge dictates the desired PWM is used to control the capacitor charge current. Switches S2 and S4 PWM pulses are applied to them. The OSIGC output voltage (VDCbus) is the capacitor's maximum charging voltage. The only purpose of the OSIGC output power during state-I is to charge the capacitors. The voltage at the load (VOAC) is zero, while the voltage across the DC bus is VDC.

State-II: in this state, the MLI input voltage (VODC) is maintained as the voltage across the DC bus. Figure 3(b) depicts the analogous circuit state l of state-I. Depending on the output voltage, positive or negative group switches are operated by switch S4 and the inverting circuit during this state. To improve inverter performance, sinusoidal pulse width modulation (SPWM) control is applied to inverters.

Switching pulses are applied to positive or negative groups in 1 phase, 2 level inverters, which typically contain 2 limbs and two serially coupled switches on each limb. The load is associated among the limbs, each of which is exposed to a DC bus voltage. The DC bus voltage is constant and switches in common inverters are straight measured by sinusoidal PWM. Since the envisioned multi level inverter DC voltage ranges from 0 to 4 VODC, SPWM control is only applicable to inverting circuits. The voltage supporter circuit of the planned Multi level inverter then employs SPWM. Shift S4 is subjected to sinusoidal PWM.

State-III: in this state, the DC bus (DC) kept at a 2 VO voltage. The DC bus has been crossed by the capacitor CI2 and the total input DC voltage (VCI2). In the circuit corresponding of state-III, revealed in Figure 3(c), shifts S2, S3, and the related circuit reversing switches are all operational. The CI2 is located

among the input of the inverter and the DC bus. As VCI2 is settled (DC), voltage across the CI2 is equal to VO. In order to power the load while the voltage across the DC bus was 2 VODC, OSIGC and capacitor CI2 were in charge. To sustain the voltage transverse the DC bus in the range among VODC and 2 VO, SPWM pulses were applied to switch S2 and S4 (DC).

State-IV: in this state, the DC bus (DC) voltage is kept at 3 VO. The input DC voltage plus the combined voltages of the capacitors CI1 (VCI1) and CI2 (VCI2) cross the DC bus. In the circuit corresponding of state-IV, which is revealed in Figure 3(d), switches S1, S4, and their related Inverting circuit switches are actuated. CI1 and CI2 are linked in series from the inverter's input to the DC bus. The capacitors in charge of supplying load power are CI1, CI2, and OSIGC. Over the DC bus voltage, VCI1, VCI2, and VODC are combined and kept at 3 VO (DC). The CI1 and CI2 capacitors are discharging. Switches S1 and S2 are subjected to SPWM pulses in order to regulate the voltage of the AC load. The range of the DC bus voltage is 2 VODC to 3 VO (DC).

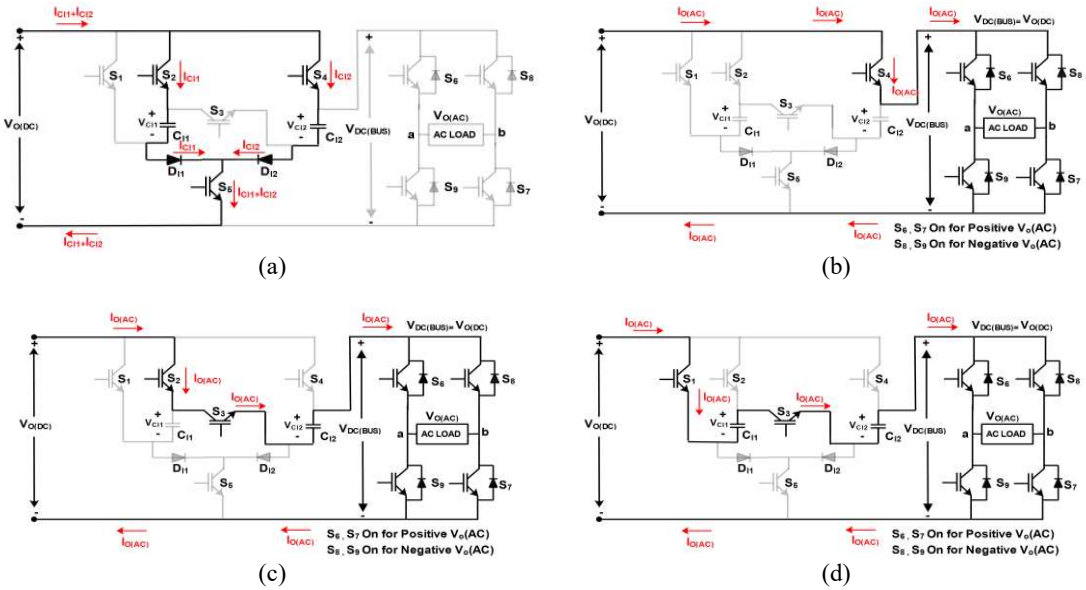


Figure 3. Multilevel inverter equivalent circuit: (a) stage 1, (b) stage 2, (c) stage 3, and (d) stage 4

4. ANALYSIS OF PROPOSED OSIGC AND MLI SYSTEMS

The OSIGC and MLI stages make up the suggested system. The inductor average voltage at stable state is assumed to be zero, and to calculate voltage gain (CCM), the OSIGC is run in continuous conduction state.

$$\frac{di}{dt} = \frac{V_{PV}}{L_1}.kT \tag{1}$$

Where T is the period, duty cycle k, and V_{PV} is input voltage of the OSIGC converter. Change in inductor current during state-II operation is expressed as (2):

$$\frac{di}{dt} = \frac{(V_{0(DC)} - V_{PV})}{L_1}(1-k)T \tag{2}$$

In (1) and (2), where output voltage V_0 is the of OSIGC.

$$V_{PV}.k = (V_{0(DC)} - V_{PV})(1-k) \tag{3}$$

In order to find the steady state voltage gain, (3).

$$\frac{V_{0(DC)}}{V_{PV}} = \frac{3-2k}{1-k} \tag{4}$$

Figure 4 the findings indicate that at any duty cycle, OSIGC has a higher voltage gain than other converters.

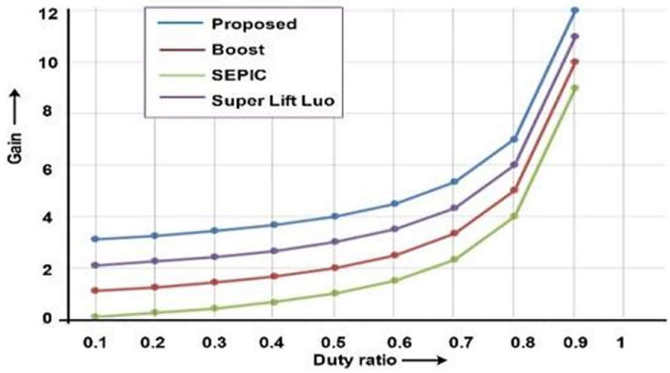


Figure 4. Comparison of the proposed OSIGC's voltage gain with the boost, SEPIC, and Luo converters

5. SIMULATION AND EXPERIMENTAL RESULT

Suggested OSIGC and MLI system's superiority is evaluated using hardware and MATLAB simulation. A 200 W load is used for experimental analysis. The OSIGC converter receives DC power from a 24 V, 200 W module. To verify that the PV module is using its maximum amount of electricity, a modified P&O maximum power point tracking (MPPT) approach is used. A IGBT with a 25 kHz frequency was used in the development of the OSIGC. Results for the OSIGC PV input voltage (VPV) and current (IPV) are displayed in Figures 5 and 6. OSIGC's input DC voltage is kept at 24.12 V, and its input current is 8.12 A. The module's PV isolation level is fixed to standard temperature is 249 ºC, and the OSIGC converter is receiving 200 Watts of electricity. Owing to MPPT, a minor change in input voltage and current has occurred.

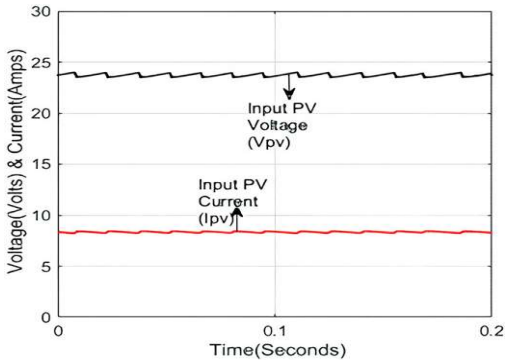


Figure 5. OSIGC input voltage and current simulation

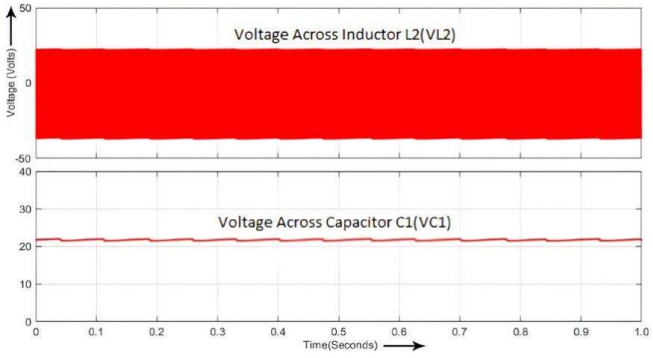


Figure 6. Across L2 and C1 voltage

The L1 and L2 values are selected as 100 mH and the C1 is 200 uF, 63 V are used. The voltages waveform across the L1, L2, and C1, are shown in Figure 6. At state-I, the voltage across L1 and L2 is positive. Inductors L1, L2, and C1 store PV energy for the duration. At state-II, the voltage across L1 and L2 is negative. Inductors L1, L2, and C1's stored energy is transmitted to the load during this time. Voltages that are always positive cross the currents through the inductors and capacitor. The charging and discharging voltages of the inductors are same. The performance of the OSIGC's voltage gain degrades due to variations in capacitor voltage Vc1 during operation. Figure 7 displays the output voltage and current waveforms of the OSIGC. In OSIGC, MPPT algorithms are run at a duty ratio of 0.6. The OSIGC has benefited.

$$\frac{V_O}{V_{IN}} = \frac{3-2K}{1-K} = \frac{3-2(0.6)}{1-0.6} = 4.5 \quad (6)$$

The gain of the OSIGC is 4.5 and the input VPV voltage is 24 V. The output current and voltage are 109 V and 1.7 A, respectively. It uses a 1000 uF, 200 V filter capacitor. The proposed OSIGC efficiency and power curves for the MPP constraint are shown in Figure 8. The output port power of OSIGC is 185 W, while the solar power input is 200 W. The OSIGC converter has an efficiency of 92.5%. Figures 9(a) and (b) shown output load voltage, current across the load are. In together cases, voltage and current at the load are in phase. The output voltage varies very slightly as a result of the capacitors' voltage fluctuations during discharge.

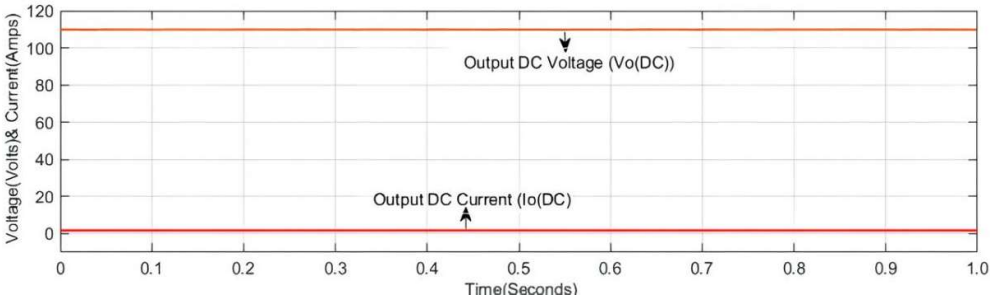


Figure 7. OSIGC output voltage and current

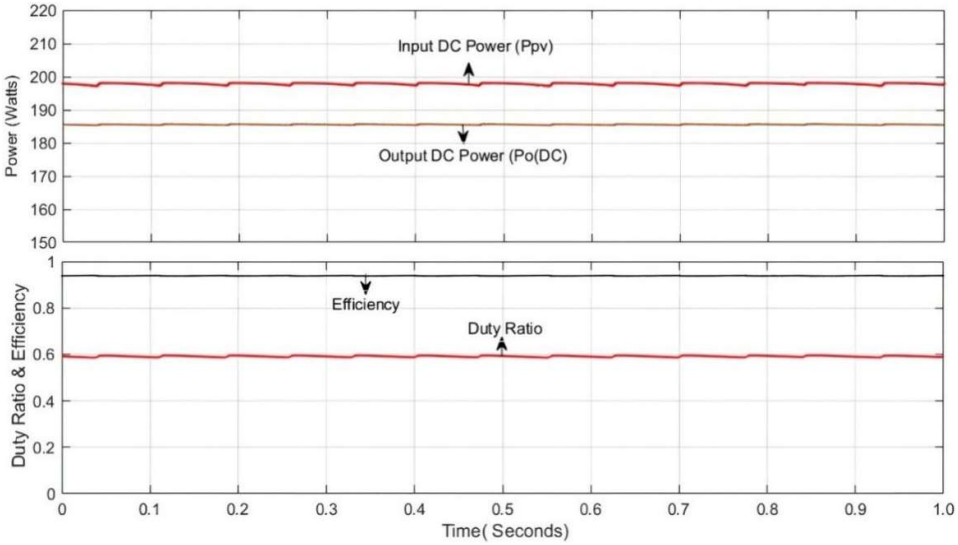
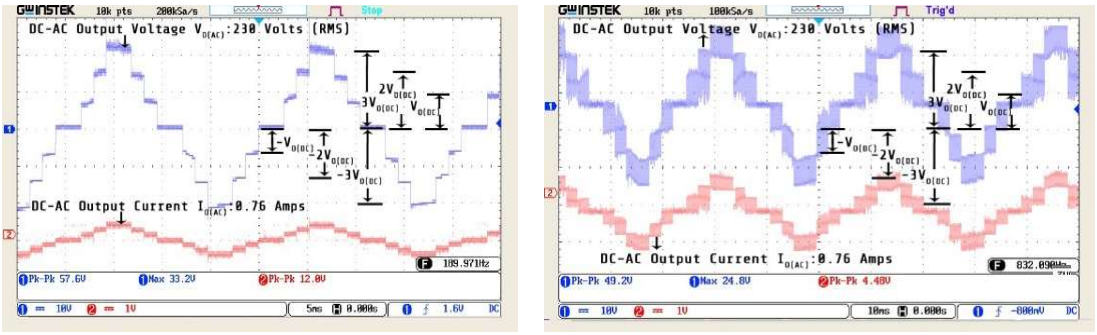


Figure 8. OSIGC power, efficiency and duty ratio

Output power of the DC-AC inverting system must adhere to IEEE Std 519. When designing DC-AC inverters, the THD value as a percentage is crucial. To drive all types of AC loads, the voltage and current must be less than 5% THD. Unwanted elements like harmonics and power quality problems are produced by higher THD values. The proposed inverter undergoes THD analysis, and the results are displayed in Figure 10.

The consequences demonstrate that the THD value is 0.182% once it has supplied a resistive load with AC power.



(a) (b)

Figure 9. Voltage and current: (a) switching pulse at constant and (b) sinusoidal PWM

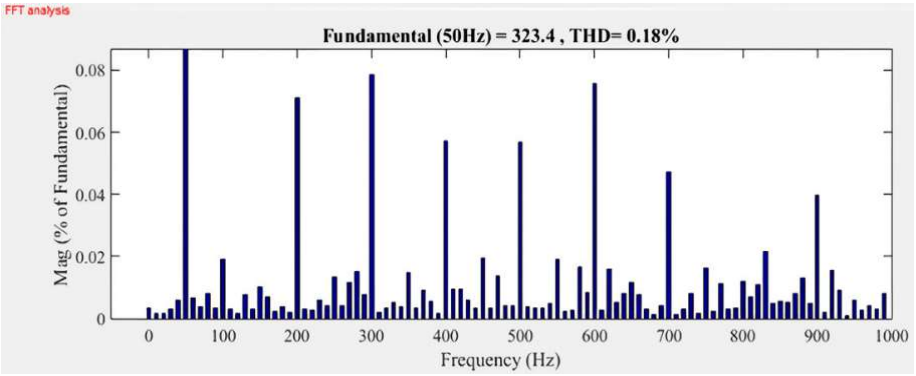


Figure 10. THD analysis of load voltage

6. CONCLUSION

A suggested improved gain converter. Both DC to DC and DC to AC conversions result in gain. The relevance of suggested OSIGC is demonstrated by the comparative gain analysis. To extract the most power possible from PVM, P&O algorithm is utilised. MLI receives the output of the DC to DC converter. The proposed inverter produces seven-level AC output and has a unique future of triple voltage gain. The inverter circuit employs the switching capacitor approach to increase voltage gain. The suggested system will be validated using the hardware prototype. The results of theoretical analysis and simulation are utilised to support the experimental findings. To enhance the AC voltage's output quality, inverter is controlled using the SPWM approach. The DC-DC converter's highest voltage gain is 12, whereas the DC to AC inverter's is 3.12. The proposed system's overall voltage gain is 36. The DC-DC converter's efficiency is 92.15%, while the DC-AC inverter's efficiency is 93%. The system's overall effectiveness is 86.12%. The AC output's THD is 0.182%. The proposed DC to DC to AC converter's key benefits include its straightforward topology, good MPPT control handling, and voltage gain gained in both the DC to DC and DC to AC stages. Both independent and grid-connected PV-based systems can use the proposed DC-DC-AC technology.

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