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New control scheme for a dynamic voltage restorer based on selective harmonic injection technique with repetitive controller

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ABSTRACT

Repetitive controller and selective harmonic injection technique (SHI) in medium and low voltage distribution networks improve dynamic voltage restorer (DVR) DC bus voltages as well as nullify power quality (PQ) problems. DVRs use sinusoidal pulse width modulation (SPWM) firing control, but DC bus use seems to be limited, affecting density, cost, and power packaging. By adding 1/6th of the 3rd harmonic waveform to the basic waveform, SPWM yields the developed model. According to the findings, 15% of DC bus usage improves and produces high voltage AC. Nevertheless, just control systems perturb PQ. The proposed controller uses feed forward and feedback to enhance transient response and justify stable zero error. 3rd third harmonic injection pulse width modulation (THIPWM) improves total harmonic distortion (THD) in the proposed scheme. Power system computer aided design (PSCAD) simulation produced high accuracy for THIPWM and repetitive controllers.

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1. INTRODUCTION

The quality of electrical power and disruptions in the power signal has become serious problem among electrical power suppliers and customers. Continuous monitoring of power is intended to enhance the power quality (PQ) which is delivered at the customer's site. Thus further, it is highly desirable to detect PQ disturbances (PQD) and a proper description of PQD [1]–[3]. Two somewhat distinct characteristics of all PQ issues are present such as energy and total harmonic distortion [4], [5]. The PQD is recognized to regularly the V_{sag} due to a switch on abnormal conditions in the network [6], [7]. V_{swell} is less common in distribution networks owed to switch on capacitive load. Harmonics due to non linear loads like furnaces and electronic devices [8], [9]. This PQD causes process shutdown which leads to financial loss. Various conventional methods are used to reduce the V_{sag} but by far the most effective approach is FACTS devices [1], [10]. Dynamic voltage restorer (DVR), distributed static compensator (DSTATCOM), static synchronous compensator (STATCOM), synchronous series compensator (SSSC), and static VAR compensator (SVC) are the flexible alternating current transmission systems (FACTS) devices that are increasingly being used to

minimize V_{sag} and other PQD [10]–[14]. The important continuation of this paper is to use repetitive controllers to formulate a governing arrangement for DVR and mitigate PQ problems. Besides that, the authored DVR customs device has been facilitated by a proportional integral (PI) controller which substitutes network voltage frequency [15], [16]. An uncomplicated mechanism is adequate to allow the reduction of voltage and to compensate for those fairly unbalanced voltages. Still, when traded with a high concert application it flops therefore, intricate controllers added are compulsory [17].

According to Nielsen *et al.* [18], the limitation of such a method is that it requires a completely autonomous filter that diminishes the independent harmonic [7]. Feed forward +PI controller feedback has been used [16] to restore the regulate global concert while being aware of a variant of the t_0 measured strategy in addition to the filter output constraint. As it can alleviate all 4 abnormalities, the framework becomes relatively simple as well as adaptable [17]. It consists of a feed forward cycle to increase the transient state and a feedback cycle to enable zero error. It could simply be done unbiasedly with such a t_0 in digital signal processing [18], [19]. In recent decades, research in V_{sag} assessment might have concentrated on creating protocols as well as methods for evaluating the disturbance [20]–[22]. There has been very little research into the causes of V_{sag}. For the remediation of PQ problems, numerous pulse width modulation (PWM) methods have been employed in DVR [23], [24]. In the existing crisis, analysts have been employing the selective harmonic elimination pulse width modulation (SHEPWM) and space vector pulse width modulation (SVPWM) strategy for DVR [25]–[27]. Even so, no dependable and technically proficient technique of implementation in an effective way is available at this time. In the sinusoidal pulse width modulation (SPWM), limited accessible voltage has been found, which would be critical for cost and power compactness excellence [28]. This will primarily address the vital third harmonic injection (THI) and it will be better to implement. The resulting flattened upper surface output signal tolerates completed modulation while retaining an estimable harmonic band [29]–[31].

In this article following points have been discussed. Section 2 describes the DVR framework and repetitive controller, in section 3 a DVR with SPWM repetitive control technique is employed. In section 4 the third harmonic injection pulse width modulation (THIPWM) DVR methodologies are intentional. Considered in designing to simulate the repetitive controller along with the parameters for information are provided in sections 5 and 6 performance with proposed control strategy with conclusion explained.

2. DYNAMIC VOLTAGE RESTORER AND REPETITIVE CONTROLLER

The system configuration includes a DVR control circuit and power circuit shown in Figure 1 a perceptive load, which includes linear and non-linear loads is added to the system. The DVR has so far been mainly comprised of a voltage sourced converter (VSC) hooked up to the AC configuration through a voltage transformer (VT), with said contact network presented in Figure 1 among supply and differentiated loads. Figure 2 seems to be simply a reflection of the respective circuit depicted in Figure 1. In which acronyms details are given in the nomenclature part. Perceptive load voltage as (1):

$$v(t) = V_{pcc}(t) + u(t) - Ri(t) - L\frac{di}{dt} \quad (1)$$

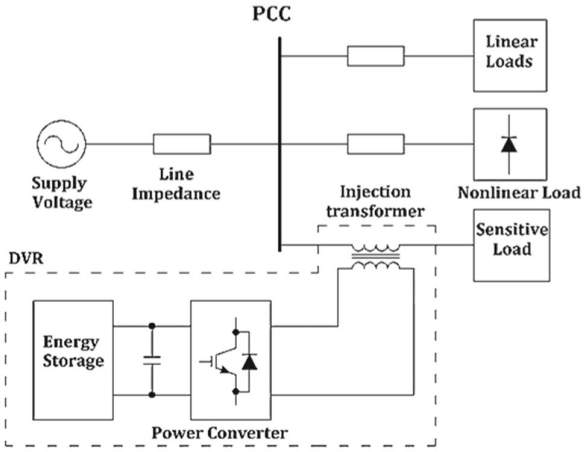


Figure 1. Basic block diagram of DVR with various loads

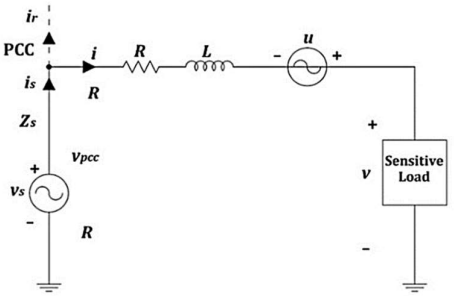


Figure 2. Equivalent DVR circuit with perceptive load [6]

Once periodic signals must be accompanied or denied, an resistor capacitor (RC) is an attempt to control way is to ensure in the internal model theory (IMP). A generic periodic signal with the ability to IMP seems to have the aforementioned shape. Figure 3 depicts a basic repetitive controller reorientation. The primary goal of a repetitive controller would be to verify that the reference of periodic trajectories has been monitored or that repeated disruptions are denied in a continuous system [29], [30].

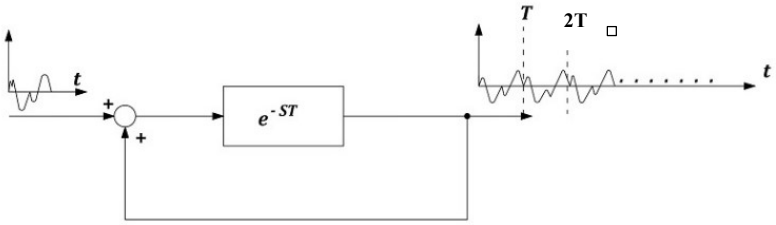


Figure 3. Repetitive controller reorientation [27]

3. PROPOSED METHOD

An essential duty of the DVR is to manage the V_{load} under the observation of different sorts of disruption. Throughout this article, the suggested closed loop control setup has been premised to make sure accurate results in a steady state condition. A prolonged time full closed loop DVR optimization approach is demonstrated in Figure 4. P1(s) has been the total amount of 1 sample period and the t_0 of the inverter implicated in PWM transitioning. Those philosophies should be computable, and the design should be easily enlarged for the three phase base. The output that's also adhered to the load is as tries to follow:
A DVR control system, *C(s),* has been as (2):

$$C(s) = \frac{M(s)}{1-e^{-\frac{2\pi}{\omega_1}s}} \tag{2}$$

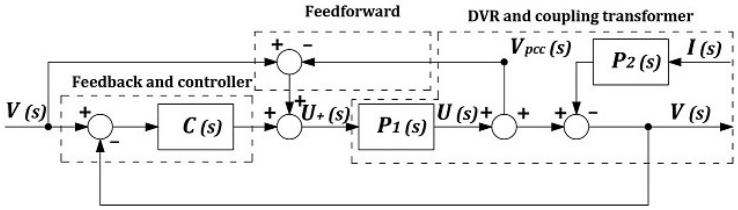


Figure 4. DVR control scheme

In which *M(s*) has become a favored term frequency (TF), ensuring stability. Takeover (2) [15]:

$$F(s) = \frac{\left[1-e^{-\frac{2\pi}{\omega_1}s}+M(s)\right]P_1(s)}{1-e^{-\frac{2\pi}{\omega_1}s}+M(s)P_1(s)} \tag{3}$$

$$F_w(s) = \frac{[1-P_1(s)]\left[1-e^{-\frac{2\pi}{\omega_1}s}\right]}{1-e^{-\frac{2\pi}{\omega_1}s}+M(s)P_1(s)} \quad (4)$$

$$F_i(s) = -\frac{\left[1-e^{-\frac{2\pi}{\omega_1}s}\right]P_2(s)}{1-e^{-\frac{2\pi}{\omega_1}s}+M(s)P_1(s)} \quad (5)$$

The attribute would be supplanted by *j* when determining the frequency response from (3) to (5). To assist in resolving the origin of complexity caused by certain parts that are modeling errors, time delay, and dead time due to inverter issues. The control system (2) could be changed as (6):

$$C(s) = \frac{Q(s)e^{-(T-\hat{t}o)s}}{1-Q(s)e^{-T}} \quad (6)$$

Q(s), pass filter TF [9]; $\hat{t}o$ is indeed a for the DVR delay, with T=2 $\pi/\omega 1$, as well as β an approach limitation that is lower than the network voltage time frame ($\beta < (2\,\pi)/(\omega 1)$). By modifying (6) throughout [16].

$$F_w(s) = \frac{[1-e^{-t_o s}][1-Q(s)e^{-Ts}]}{1+Q(s)e^{-Ts}(e^{-\delta s}-1)} \quad (7)$$

$$F_i(s) = -\frac{[1-Q(s)e^{-Ts}]P_2(s)}{1+Q(s)e^{-Ts}(e^{-\delta s}-1)} \quad (8)$$

with, $\delta = t_o - \hat{t}_o$.

3.1. Third harmonic injection pulse width modulation strategy in a dynamic voltage restorer

The SPWM technique has been used for DVR in the majority of investigations. Even so, the utilization of the dc bus has been insufficient in the SPWM. The goal of such an approach becomes to enhance the $V_{L\text{-}L}$ of a PWM inverter by 15% without the need for a pulse drop modulation scheme. Because of the incorporation of 3rd, 9th, and 15th harmonics, in which amplitudes are 1/6th and 3rd harmonics decided to add to the sinusoidal waveform [29], [30]. Such harmonics feed on the ground toped phase waveform, which improves inverter effectiveness, but castoffs have been castoffs in today's high scheme and have been initiated in this technique, which concentrates on IGBT DVR. The 3rd harmonic scale function is stated to be capable of making a phenomenal change to the inverter's output phase waveform given (9).

$$y = sin\,\omega\,t + A\,sin\,3\,\omega t \quad (9)$$

From which *A* is recognized as *y* optimal value, this could be expressed as (10).

$$\frac{dy}{dt} = cos\,\omega\,t + 3A\,cos\,3\,\omega t = 0 \quad (10)$$

As a result, the waveform's maxima and minima occurred at (11) and (12):

$$cos\,\omega\,t = 0 \quad (11)$$

$$cos\,\omega\,t = \frac{(9A-1)^{1/2}}{12A} \quad (12)$$

In (9) becomes:

$$y = (1+3A)\,sin\,\omega\,t - 4A\,sin^3\,\omega\,t \quad (13)$$

$$y = sin\,\omega\,t + \frac{1}{6}sin\,3\,\omega t \quad (14)$$

To show that no more inclusion in by summing of triple harmonics seems to be feasible, the values of *t* over which mountain ranges of *y* occur are initiated by modifying (11) and (12). As expected, (11) yields ωt=π/2 independent of *A*, and yet (5) yields:

$$cos\,\omega\,t = \frac{1}{2} \quad (15)$$

i.e., $\omega t = \pi/3, \omega t = 2\pi/3$ (16)

Those triple harmonics surpass *0* throughout all ωt statistics. Thereby, bringing triple harmonics did not affect the additional fall $\hat{y}$, as well as the special hypothesis, is accurate. $\omega t = n\pi/3$ in (14), find the maximum values of y.

$$y = \pm\frac{\sqrt{3}}{2} \quad (17)$$

and, $\hat{y} = \pm 0.866$

Essentially, 2/3rd is the reference sinusoidal waveform, and by including a 3rd harmonics aspect whose magnitude has been 1/6th of the original input waveform, the peak value of output has been reduced by an element of 0.866 without modifying the fundamental amplitude. One such technique has been depicted in Figure 4; a component here raises the modulating wave magnitude, allowing the inverter's absolute V_{max} to be applied once more. In addition to modulating waveform in (18):

$$y = K\left(sin\,\omega\,t + \frac{1}{6}sin\,3\,\omega t\right) \quad (18)$$

Let's assume no least pulse width threshold exists, y has been attributed to 1. According to the waveform seen in Figure 5, the maximum value of y=0.866. The sum of 1/6th of the 3rd harmonic findings in such a 15.6% rise is in the amplitude of the fundamental phase voltage waveform [31] and thus in the load voltage waveform as shown in Figure 5.

$$1 = K \times 0.866 \text{ and } K = 1/0.866 = 1.15 \quad (19)$$

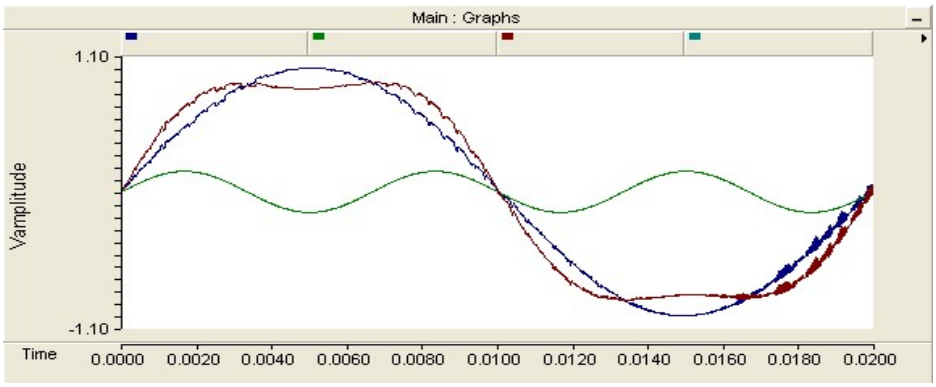


Figure 5. Rising a basic V_o by 1/6th of the 3rd harmonic reference peak=0.866 and fundamental magnitude=1

4. METHOD

The DVR topologies with various loads shown in Figure 1 and the RC closed loop strategy of control for DVR shown in Figure 4 were simulated in power system computer aided design software, as shown in Figures 6-8 respectively. The test system consists of a 400 V, 50 Hz, three phase source feeding three separate loads i.e., induction motor, nonlinear load three phase rectifiers, and three phase perceptive rectifiers. A DVR has been linked in between point of common coupling (PCC) and the delicate load via a 20 kVA transformer with a unit turns ratio as well as a secondary coil bushed to the star. The V_{dc} storage device has been 400 V SPWM. Table 1 tabulated system parameters and controller parameters of the DVR system.

To appropriately architecture the controller attribute, a monetary value for the t_0 has been chosen within a specified range [29]. The PWM has been responsible for the t_0. SPWM can be used in any subheading to generate switching pulses for the controller, being a three phase conversion. For each phase, a controller was configured using a coordinating scheme of three phases *a, b,* and *c*. Maybe, if operating under

imbalance situations, the references frame a, *b,* and *c* has become the most prevalent solution to the regulation of load voltage.

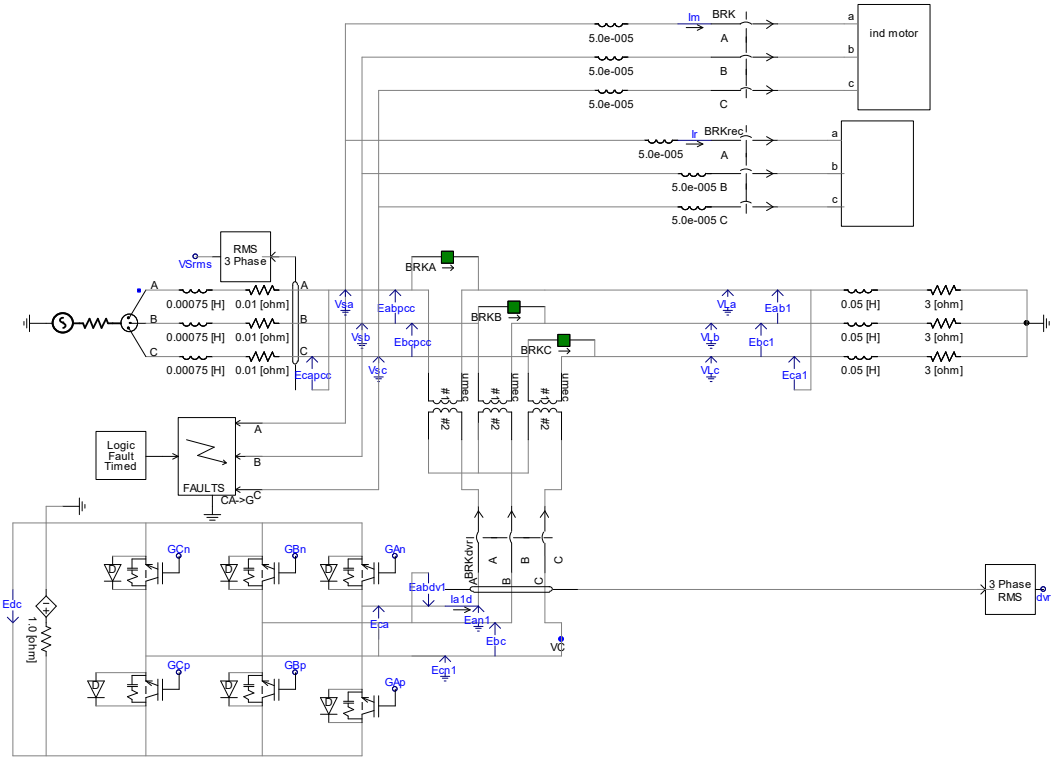


Figure 6. The study system developed in simulation software

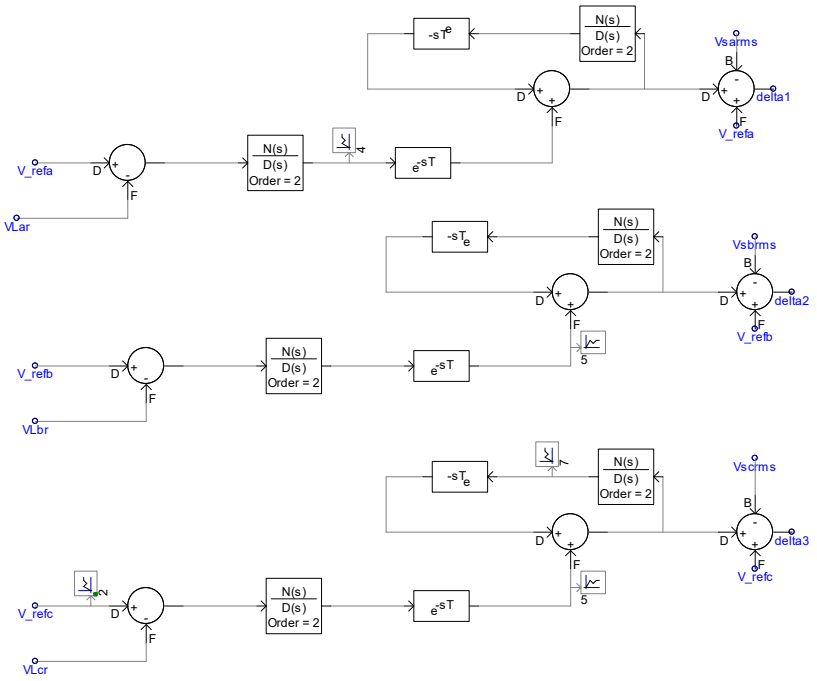


Figure 7. Repeatable controller applied in PSCAD

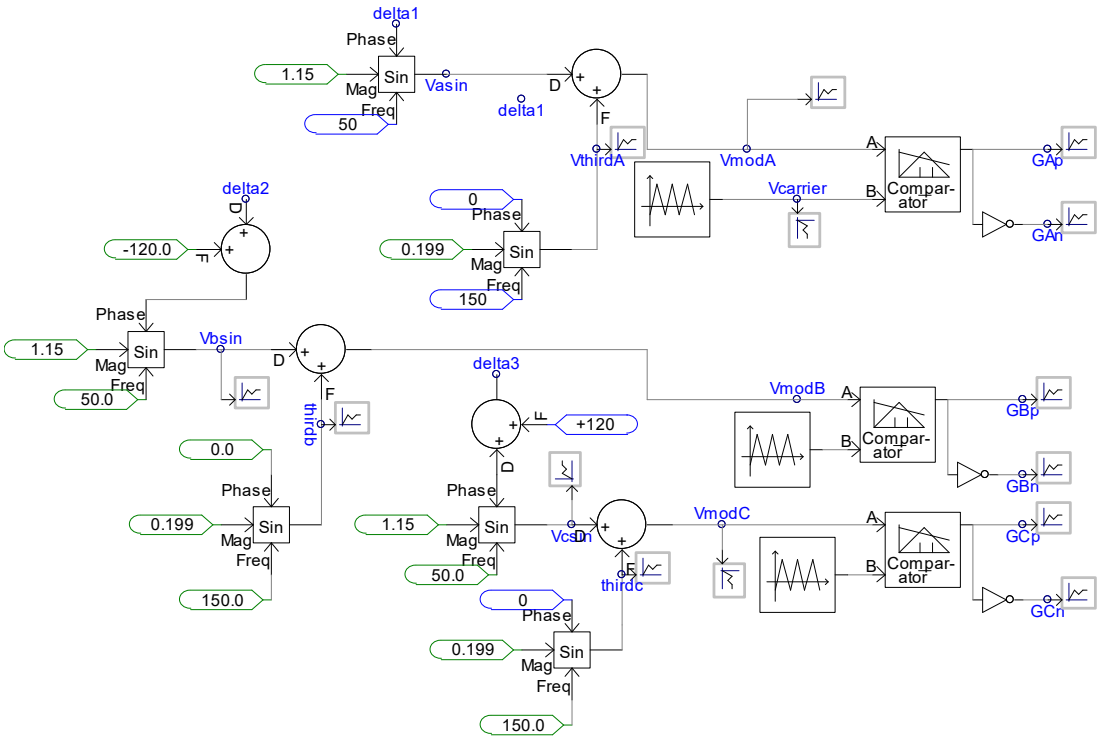


Figure 8. The software incorporates the THI approach for DVR

Table 1. Test system and controller parameters

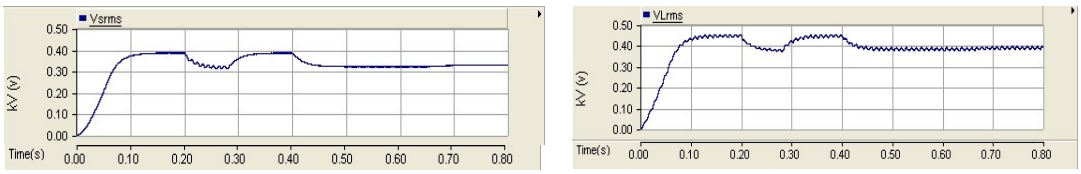
Study system parameters		DVR controller parameters	
Parameter	Value	Parameter	Value
$V_{RMS\ L\text{-}L}$	5 Hz	Switching frequency (f_s)	6.45 kHz
R and L of the distribution line	R_s=10 mΩ, L_s=750 µH	Frequency- modulation Index (m_f)	27
Motor inductance	L_l=50 µH	DVR delay (t_0)	1/2 f_s
Resistance and inductance of the DC load	R_{dc}=10 Ω, L_{dc}=0.4 H	δ	0.2 t_0
Perceptive load: resistance and inductance	R_{sl}=3 Ω, L_{sl}=50 mH	Amplitude modulation index (m_a)	0.8

5. RESULT AND DISCUSSION

The simulation circumstance in the discrete shown in Figure 6 where the simulation was performed is as follows. The simulations are represented as nonlinear load trails and the DVR is coupled at $t = 0$ s, L-G fault is generated at PCC from $t = 0.2$ s to $t = 0.28$ s through an $Rf = 0.3$ Ω.

5.1. Sinusoidal pulse width modulation computation with resistor capacitor

At PCC, the V_{RMS} is initially 381 V and when the *L-L* fault becomes practical this falls to 316 V. When the Induction drive is associated at *t*=0.4 s, the V_{PCC} falls to 336 V trying to instigate V_{sag} by 16% w.r.t. the present value. Towards the end the nonlinear charge is isolated towards *t*=0.65 s and at the PCC the voltage rises to 350 V. Figures 9(a) and (b) demonstrates an estimate of V_{LRMS} and V_{SRMS} that the DVR could deliver 400 V at responsive load, as well because of the various variations in voltage at PCC.

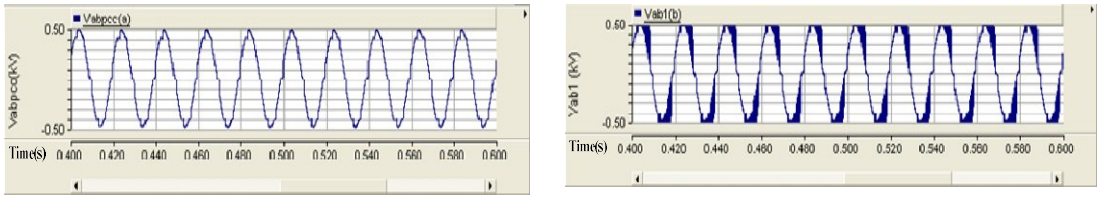


(a) (b)

Figure 9. *3ϕ* RMS voltage; (a) Vs_{rms} at PCC without DVR and (b) V_{Lrms} at perceptive load with DVR

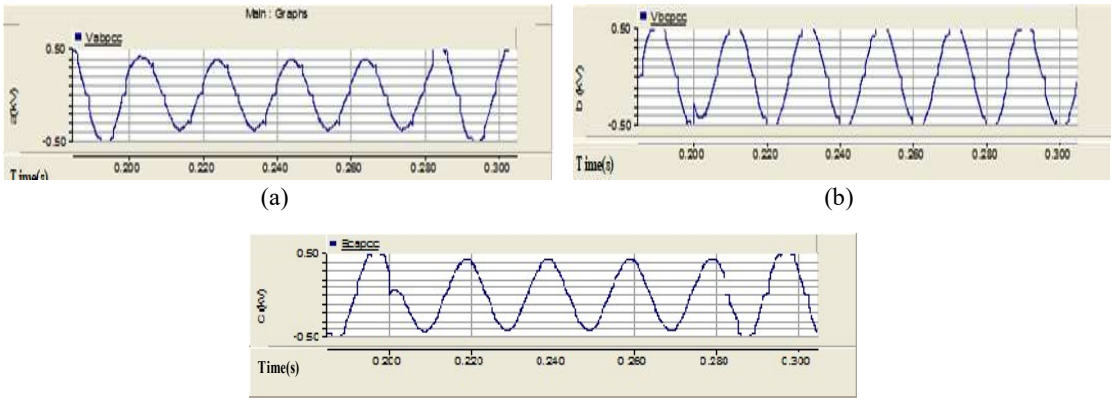
Figures 10(a) and (b) show outcomes in the case of nonlinear load and perceptive load contact alone, with an interference time of 0 to 0.2 s. Figure 10(a) $V_{L\text{-}L}$ illustrations in the PCC $V_{ab}P_{cc}$, the distortion of the waveform is due to the harmonic current haggard of the rectifier, so the total current provides perceptive load and the rectifier root a drop in the PCC voltage. $V_{L\text{-}L's}$ fourier analysis indicates that the RMS value for the basic frequency=381 V and THDV=4.40%.

Illustrations of $V_{L\text{-}L}$ over delicate load as described in Figure 10(b), throughout this case, the fundamental harmonic appears to have a voltage of 403 V_{rms}, although the THD is THDV=3.27%. This harmonic distortion value was considered to be due to harmonics of high frequency that facilitate the PWM technique. The consequences gained subsequently are shown in Figures 11(a) to (c) and 12(a) to (c) of a short circuit that occurs. It is seen that t=0.2 s to the given period t=0.28 s from time interval. Figure 12 simply proves the fault and roots of an unbalanced V_{sag} and repetitive controller compensated voltages are shown in Figures 13(a) and (b). At the time of 0.4 s induction, the drive is started and this results in V_{sag} of 83% of normal PCC voltage this is exposed in Figure 13. The load voltage is improved to 99.5% using the repetitive controller.



(a) (b)

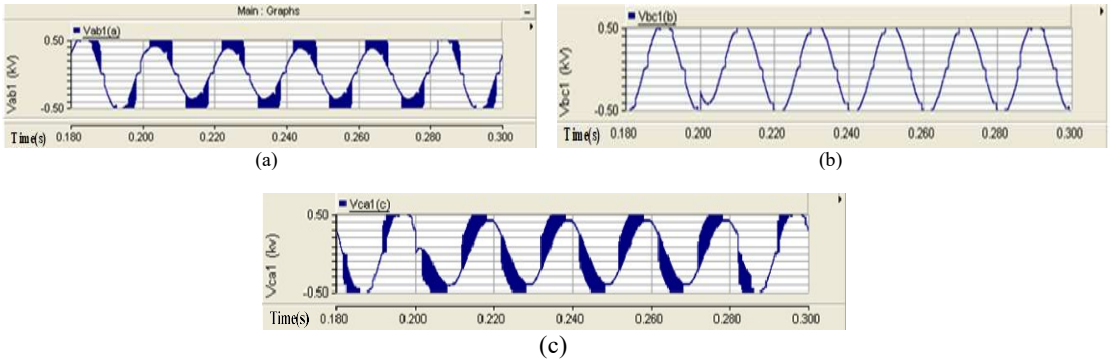
Figure 10. Line voltage; (a) at PCC and (b) across perceptive loads with DVR for consistent to the interval $0.2 \leq t \leq 0.28$



(a) (b)

(c)

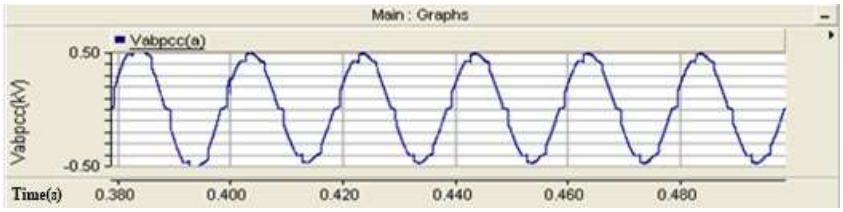
Figure 11. $V_{L\text{-}L}$ at; (a) V_{PCC} AB, (b)V_{PCC} BC, and (c) V_{PCC} CA consistent with the interval $0.2 \leq t \leq 0.28$



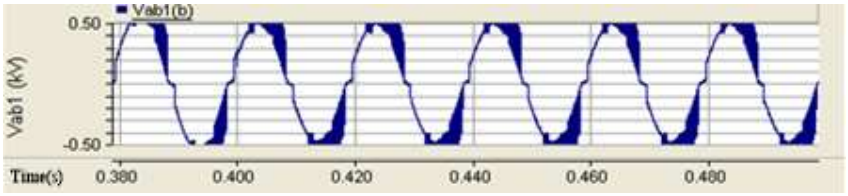
(a) (b)

(c)

Figure 12. $V_{L\text{-}L}$ at load; (a) V_{ab1}, (b) V_{bc1}, and (c) V_{ca1} consistent to the interval $0.2 \leq t \leq 0.28$



(a)



(b)

Figure 13. $V_{L\text{-}L}$; (a) at the PCC and (b) at the perceptive load consistent with interval $0.4 \leq t \leq 0.65$

5.2. Third harmonic injection pulse width modulation computation with resistor capacitor

The inclusion of a 6th of a 3rd harmonic, as depicted in Figures 14 to 17, improves the magnitude of the basic V_{ph} and thus the V_L by 15.5%. Having taken marginal constraints in pulse width into account, a significant lead to an increase in V_o seems to be possible. The $V_{L\text{-}L}$ waveform remains constant because this phase waveform nullifies the 3rd harmonic content. The V_{ph} peak of the fundamental element in SPWM is $V_{dc}/2$ as compared to 2 $V_{dc}/2$ when controlled by 6 pulses. In the SPWM methodology, the value of the V_{dc} bus has been ($V_{dc}/2$)/(2 V_{dc}/π) in other words 0.785=78.55%.

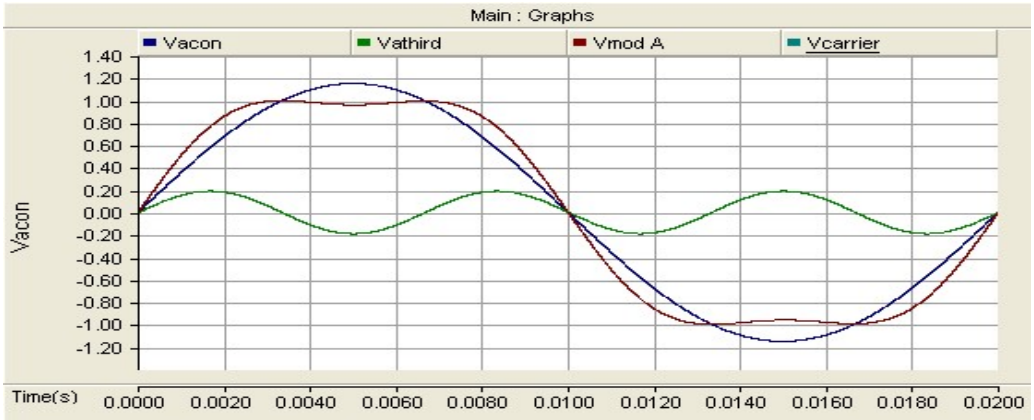
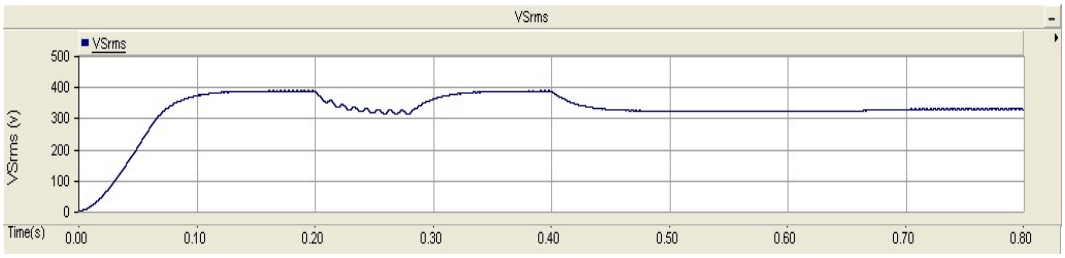
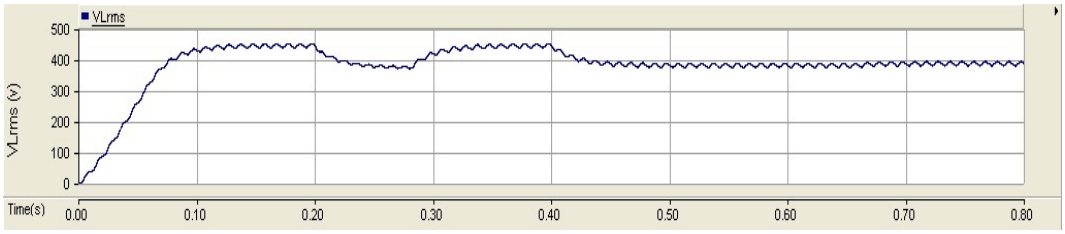


Figure 14. 3rd harmonic added to peak reference=1 and FA=1.15

The fundamental entity's V_{pn}-Peak besides THIT is 0.785*1.15=0.907 (90.07%). Figure 14 illustrates waveform orientation tilted besides having to add 1/6th of the 3rd harmonic with such a 1.15 peak sine wave reinstate particularly in comparison to the amplitude of 1. Figures 15(a) and (b) show V_{PCCRMS} and V_{LRMS} with THIPWM 285 V, in which the amplitude of the foundational has been 1.15 and indeed the reference, has been recovered to 1. Figure 16 depicts the DVR- $V_{L\text{-}L}$ with THIPWM whenever the V_{dc} bus has been set to 284 V. Once the DC bus voltage seems to be 400 V, the V_{pn}- peak using the SPWM for ma=0.8 is 282 V, which is then equated with the THIPWM method. V_{dc} bus was 325 V, at that time the fundamental peak has been 282 V, and although TPIPWM has been abridged at 285 V, V_{dc} increased by 15% in contrast to SPWM as shown in Figures 17 and 18.



(a)



(b)

Figure 15. Line voltage RMS magnitude; (a) at PCC and (b) load with THIPWM when V_{dcbus}=285 V

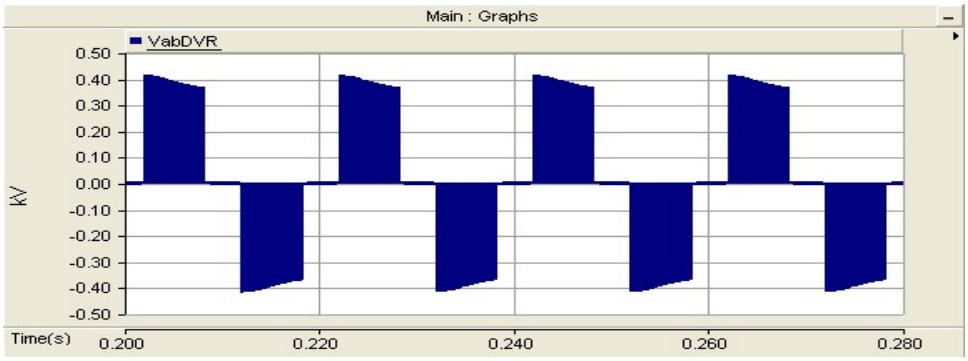


Figure 16. Line voltage of DVR supporting THIPWM (V_{dcbus}=284 V)

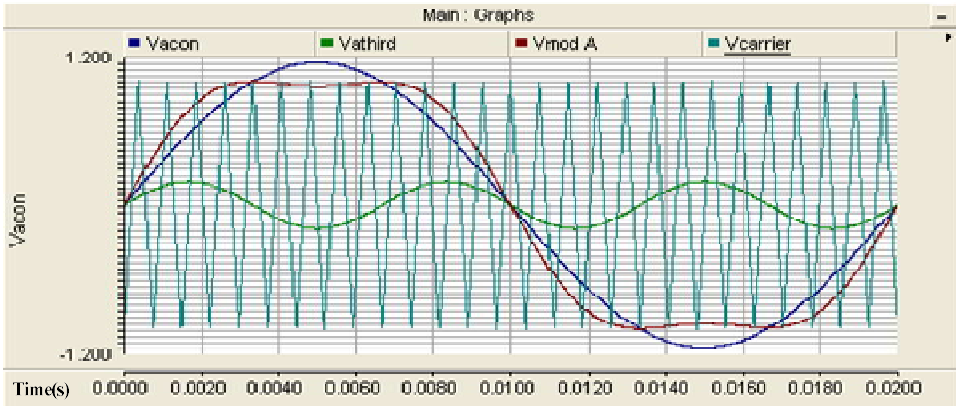


Figure 17. For 1/6th of the 3rd added harmonic and peak reference value restored to 1 peak=1, FA=1.15 phase A

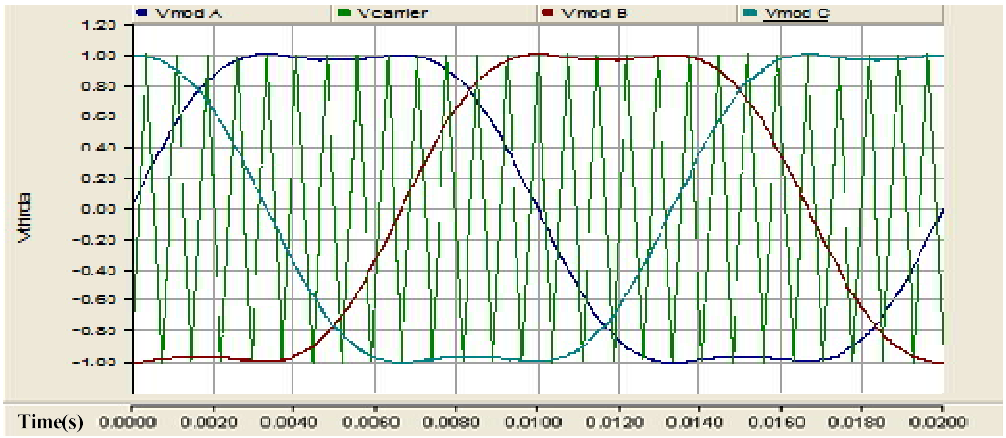


Figure 18. 3rd harmonic injected technique with a 1/6th of a 3rd harmonic applied value and a peak restored to 1, PA=1, FA=1.15

6. CONCLUSION

As discussed, in the THI method, the DVR performance has been improved from 77.6% to 91% in SPWM and THIPWM methods respectively in terms of the use of DC-bus. Consequently, the DVR rating is enhanced with the same rating of DVR. From the figures and findings, the THD comparison of SPWM and THIPWM it is observed that THD is down slightly. The main feature of the repetitive controller deals with PQD. Thus, based on the overall study repetitive controller and THIPWM technique is recommended for compensation of PQ disturbances and use of DC bus of DVR.

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