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Enhancing power conversion efficiency in five-level multilevel inverters using reduced switch topology

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ABSTRACT

This paper presents extensive research on improving the power conversion efficiency of five-level multilevel inverters (MLIs) by utilizing a reduced switch topology. MLIs have received an abundance of focus because of their ability to generate high-quality output waveforms and have better harmonic outcomes than traditional two-level inverters. The high number of switches in MLIs, on the other hand, can result in increased power losses and lower overall efficiency. In this paper, a novel reduced switch topology for five-level MLIs, which is having five switches is proposed with the aim of minimizing power losses while preserving superior performance due to lesser number of switches. To achieve efficient power conversion, the proposed topology employs advanced pulse width modulation control strategies and optimized switching patterns. The simulation results show that the minimized switch topology improves the power conversion efficiency of the five-level MLI, resulting in lower losses and better overall system performance. The total harmonic distortion (THD) value of the output current has been reduced to 7.12% and the efficiency has been achieved to 96.92%. The findings of this investigation help to advance MLI technology, allowing for more efficient and reliable power conversion in a variety of applications such as renewable energy systems, electric vehicles, and industrial drives.

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1. INTRODUCTION

Multilevel inverters (MLIs) have gained significant attention in power converter research due to their capacity to produce clean waveforms and reduce harmonic distortion, making them popular in renewable energy setups, motor control applications, and large industrial systems. The five-level inverter is a popular multilevel topology that provides better voltage waveform superior and lower switching losses than traditional two-level inverters. In the traditional five-level topology, adding more power electronic switches raises costs, complexity, and reduces power conversion efficiency [1]-[3].

A number of investigations have been conducted examining various circuit configurations, control strategies, and performance evaluation for developing proposed MLI. The diode-clamped (DC) MLI, the

flying capacitor (FC) MLI, and the cascaded H-bridge MLI are some typical MLIs that can be controlled using sinusoidal pulse width modulation (SPWM). The cascaded H-bridge (CHB) inverter has a common topology that consists of a series of H-bridge cells cascaded to generate the desired output voltage waveform. Higher voltage levels, fewer switching losses, and improved power quality are the primary benefits of the cascaded H-bridge topology. Another typical topology that uses a series of capacitors to achieve the desired voltage levels is the FC MLI. This topology is more compact, has fewer components, and produces superior voltage waveforms. Various studies, such as space vector modulation and carrier-based pulse width modulation, have offered control mechanisms for obtaining balanced output voltage while minimizing harmonic distortion. In recent years, there has been a lot of interest in the potential of a five-level MLI, notably the neutral-point-clamped (NPC) inverter. The utilization of various voltage levels to generate the desired output waveform is key to the MLI concept. The NPC inverter, in particular, offers a number of advantages, including decreased harmonic distortion, lower switching losses, and improved voltage waveform quality [4]-[8].

In MLIs, various pulse width modulation techniques, such as phase-shifted SPWM and level-shifted SPWM, can be used to improve performance. To achieve better harmonic characteristics and voltage balancing, these techniques involve shifting the reference waveform or carrier waveform. In multicarrier SPWM, multiple carrier waveforms can be used rather than a single carrier waveform. This method spreads harmonics among several carriers, reducing stress on individual switching devices and enhancing overall performance [9]-[15]. The harmonic performance of the output voltage is affected by the positioning of the carrier waveform within the reference waveform. To reduce harmonic distortion, optimal carrier disposition techniques such as phase disposition and alternate phase opposition disposition can be used. The goal of this control strategy is to remove specific harmonics from the output voltage waveform. However, selective harmonic elimination (SHE) can be computationally demanding and may not always provide a global solution [16]-[20].

Switching losses occur during voltage level transitions. The finite switching speed of power electronic devices such as insulated gate bipolar transistors (IGBTs) and metal oxide semiconductor field effect transistors (MOSFETs) is primarily responsible for these losses. To reduce switching losses in MLIs, various techniques such as pulse-width modulation (PWM) schemes and advanced control strategies have been suggested. Conduction losses occur when power semiconductor devices are in the conducting state due to a voltage drop across it. The magnitude of these losses is determined by the switch conduction losses and the output current. To reduce conduction losses in MLIs, various device technologies and circuit topologies can be used. The energy dissipated in the inductors and output filter inductors causes inductive energy losses. The losses are influenced by factors such as inductor resistance, core losses, and output current. In MLIs, optimizing inductor variables and using high-efficiency magnetic materials is a way to reduce the inductive energy losses. The requirement for a large number of voltage levels to achieve improved waveform quality is one constraints of proposed MLIs. As the number of voltage levels rises, consequently rises the number of components (switches and capacitors), resulting in raised complexity, cost, and overall system size. The number of voltage levels increases the control complexity of MLIs [21]-[25].

In order to overcome switching losses, boost efficiency, and decrease the number of switches, the following key objectives have been implemented into consideration in this paper for the proposed five level MLI: the primary objective of improving power conversion efficiency in a five-level MLI using reduced switch topology is to improve system overall efficiency. This includes minimizing power losses during the conversion process while increasing output power delivered to the load. To ensure the effective operation of the dynamic load changing, the MLI needs to generate output voltage and current waveforms of high quality. The purpose of using a reduced switch topology is to minimize switching losses during MLI operation. Switching losses can have a significant impact on overall system efficiency, and reducing these losses have been resulted in improved performance. Total harmonic distortion (THD) is a measurement of the distortion in the output voltage or current waveform when compared to a perfect sinusoidal waveform. THD has to be maintained to a minimum because high distortion can result in higher losses and lower efficiency. Sinusoidal pulse width modulation has been applied to power switches for smooth transitions between voltage levels and reduce the amount of time spent in undesirable voltage states. Based on power loss, THD, and efficiency are compared to conventional methods.

2. PROPOSED TOPOLOGY

Figure 1 depicts a conventional CHB five-level inverter with eight power switches. It consists of up of multiple power electronic switches that are cascaded together to produce a multilevel output voltage waveform. The switches in the inverter are controlled to produce different voltage levels, and each level of the device has a distinct DC voltage source. Due to the existence of eight power switches, the stair case

output waveform requires the use of eight power driver circuits. However, since the proposed topology shown in Figure 2 has five power switches, five power driver circuits are required for obtaining five level stepped output voltage pattern.

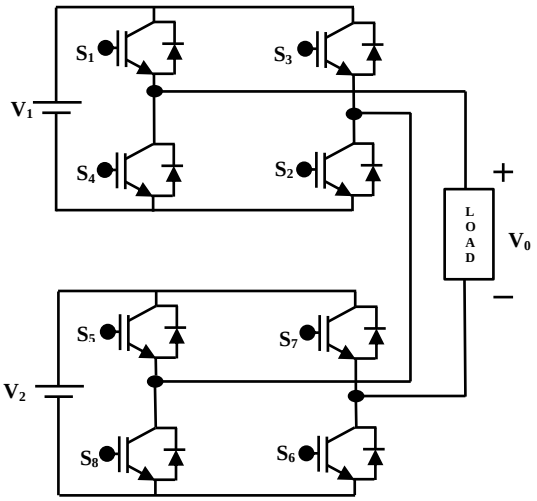

Figure 1. Conventional five level MLI

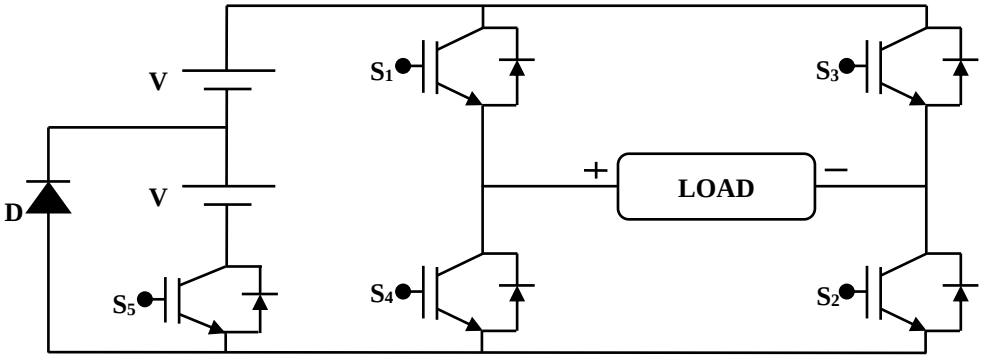

Figure 2. Proposed MLI

Figures 3-6 depicts the proposed MLI's multiple performing modes, each of which is associated with a specific output voltage switching pattern, such as +2 Vdc, Vdc, 0, -Vdc, and -2 Vdc. In the absence of any active switches, the output voltage remains constant at zero. Table 1 presents a comprehensive comparative analysis of several key parameters related to the DC supply, power switches, diodes, DC bus, and balancing capacitors in the context of three distinct MLI topologies: the DC MLI, the FC MLI, and the CHB MLI.

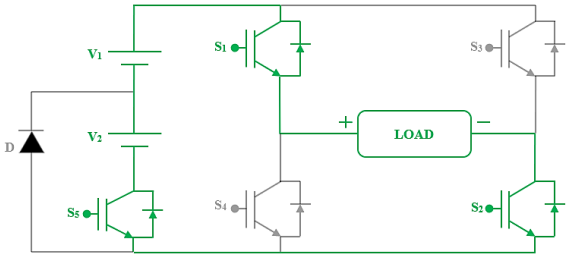

Figure 3. +2 Vdc output voltage

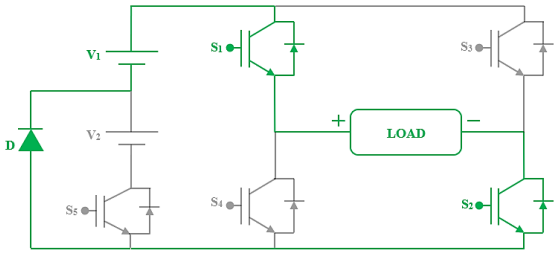

Figure 4. +Vdc output voltage

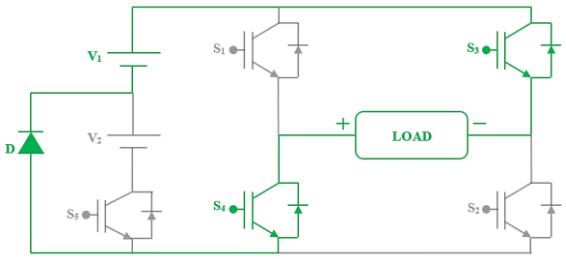

Figure 5. -Vdc output voltage

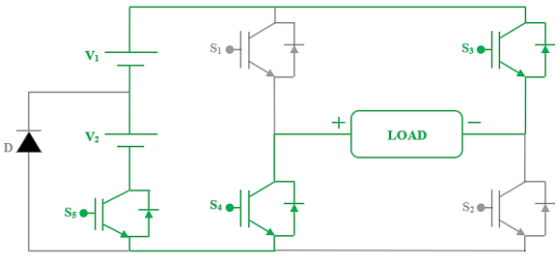

Figure 6. -2 Vdc output voltage

Table 1. Comparative components of conventional and proposed MLI

Parameters	DC	FC	CHB	[3]	[9]	[19]	Proposed MLI
DC supply	1	1	2	1	1	1	2
Switches	8	8	8	9	5	10	5
Diodes	12	-	-	-	-	-	1
DC bus capacitors	4	4	-	1	2	-	-
Balancing capacitors	0	6	-	-	-	3	-

3. PWM AND EFFICIENCY EVALUATION

In a MLI, SPWM has been used one reference waveform and four carrier signals. This method is used to generate a variety of voltage values in the output. Typically, the reference waveform represents the desired sinusoidal output voltage. The four carrier signals, which are frequently phase-shifted, regulate the inverter's switching of different voltage levels. The PWM controller adjusts the duty cycles of the switching devices to approximate the required sinusoidal waveform by comparing the reference with these carriers. This method enables MLIs to generate high-quality alternating current output with decreased harmonics, increased efficiency, and reduced voltage stress on components. Figure 7 illustrates the sinusoidal PWM technique, which is employed in proposed five level inverters.

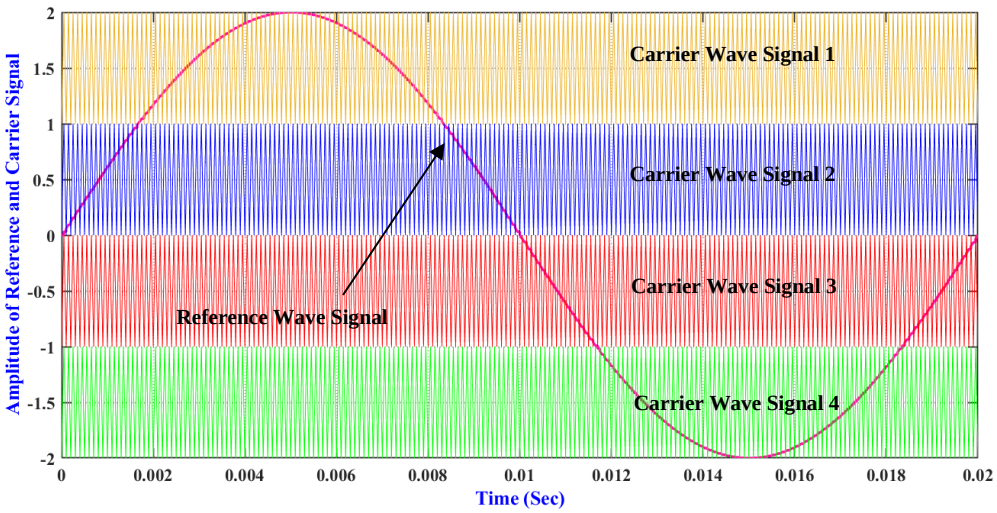

Figure 7. Sinusoidal pulse width modulation

Influences the amplitude modulation of the MLI show in (1), while (2) controls the frequency fluctuations:

$$Amplitude \quad Modulation = \frac{V_m}{V_c(m-1)} \tag{1}$$

$$Frequency \quad Modulation = \frac{f_c}{f_m} \tag{2}$$

In a modulation system, V_m represents the maximum voltage, V_c represents the control voltage, m signifies the modulation index, f_c denotes the carrier frequency, and f_m represents the maximum frequency. THD of proposed MLI has been calculated by (3). Furthermore, the current THD has been meticulously calculated, providing precise and comprehensive insights into the system's performance.

$$Total\ \ Harmonic\ \ Distortion = \sqrt{\frac{V_2{}^2+V_3{}^2+V_4{}^2+\ldots.+V_N{}^2}{V_1}} \quad (3)$$

Switching losses and conduction losses are important factors influencing total efficiency in five-level MLIs. Switching losses occur during voltage level transitions as power devices (IGBTs) switch on and off. These losses are caused by the finite switching speed and potentially produce heat loss, lowering system efficiency. Conduction losses, on the other the same direction, are generated by the intrinsic resistance of power devices when they happen to be performing. Both forms of losses are required to minimized in order to improve the performance and energy efficiency of MLIs, making them a critical concern in their design and operation. In (4) has been used to express the total power loss:

$$Total\ \ Power\ \ Losses = Switching\ \ Losses + Conduction\ \ Losses \quad (4)$$

However, the impact of efficiency calculation on power conversion performance is critical in five-level MLIs. Accurate efficiency assessments promote optimal energy consumption and minimize losses, which is critical for long-term sustainability and cost-effectiveness. Furthermore, it has an impact on component sizing, cooling needs, and overall system architecture. Efficiency is especially important in m MLIs because it reduces harmonic distortion and improves output waveform quality. Efficient operation decreases heat generation, increases equipment lifespan, and enhances system reliability, making it a critical success element for these sophisticated power electronics systems. The efficiency of proposed system is calculated by (5):

$$Overall\ \ Efficiency = \left[\frac{Output\ \ Power}{Output\ \ Power+Total\ \ Losses}\right] * 100 \quad (5)$$

4. RESULTS AND DISCUSSION

The performance of the five-level MLI has been investigated in the MATLAB/Simulink simulation and Figure 8 shows the inverter's output voltage, which is set at 230 V. Figure 9 represents the output current with resistive loads of 50, 100, 150, and 200. Figure 10 illustrates the dynamic load change output current from R to RL load. Figure 11 illustrates the output voltage with a modulation index change of 1 to 0.5; the output voltage has been reduced from five to three levels due to the lower modulation index value. Figure 12 illustrates a THD analysis of voltage and current for an RL load. As a result of inductive inference, the THD value of current is reduced by 7.12%. In Figure 13, the current THD analysis is illustrated for the RL load of both the cascaded conventional H-bridge inverter and the newly proposed inverter. Figure 14 presents an efficiency analysis comparing the proposed MLI with conventional inverters. Based on the findings, it is evident that the proposed MLI exhibits superior efficiency compared to conventional inverters, attributed to its reduced number of power switches, minimized power losses, and lower THD.

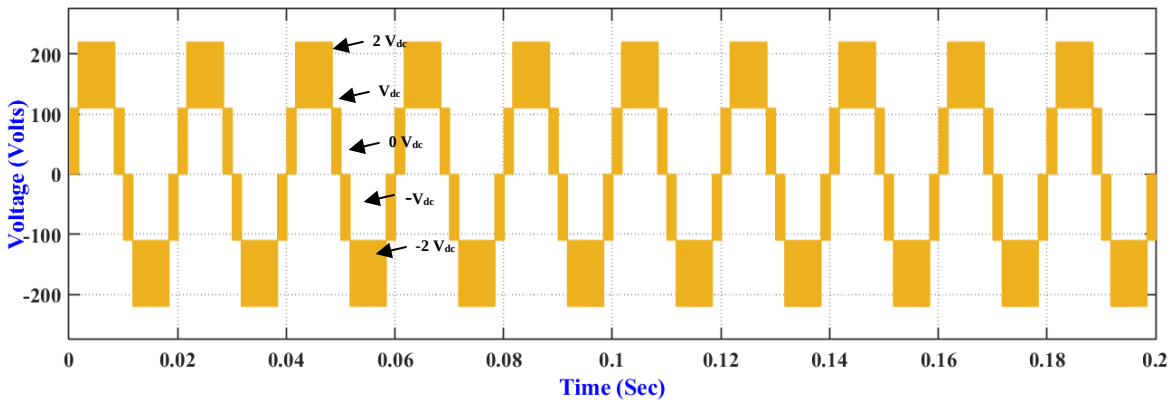

Figure 8. Output voltage of proposed five level inverters

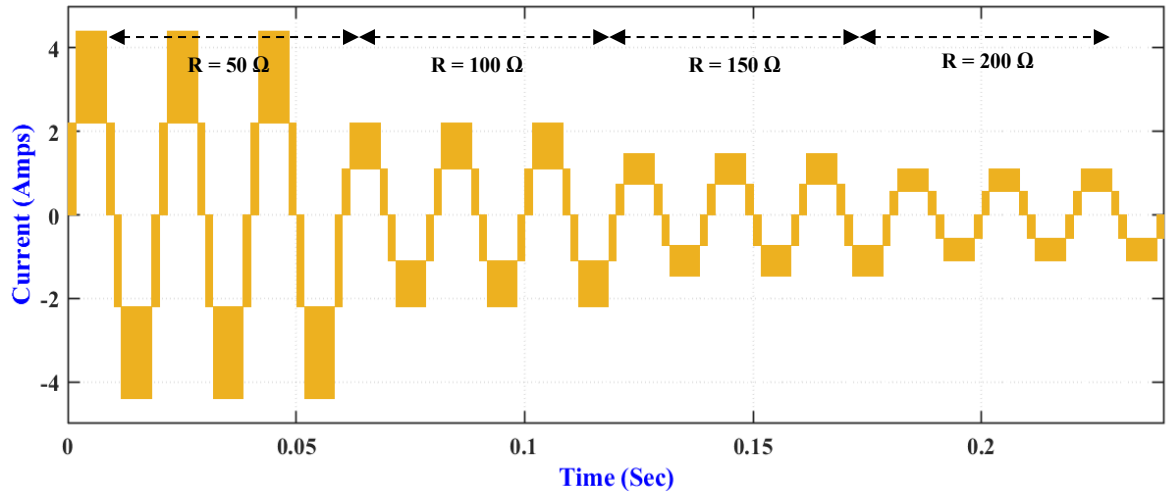

Figure 9. Output current with variable resistive loads

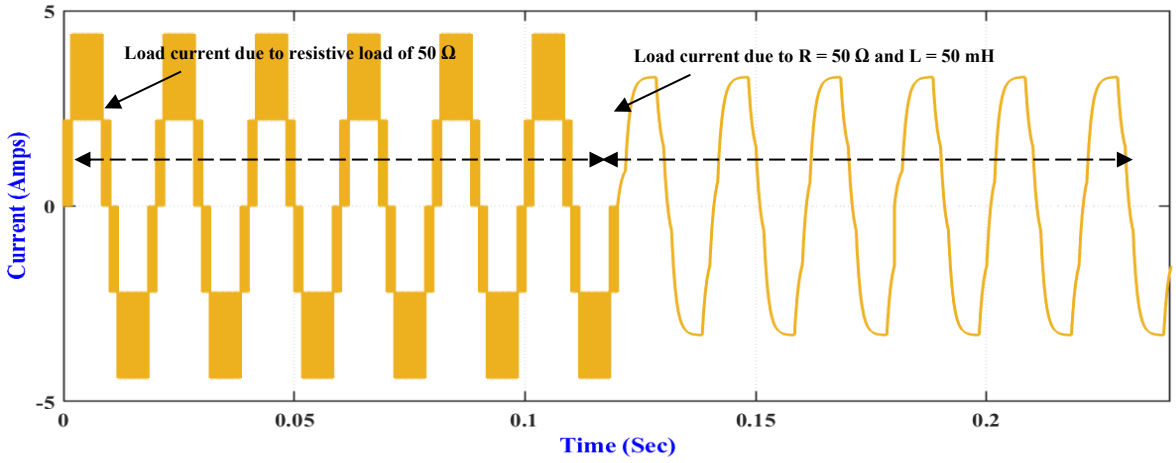

Figure 10. Output current with R to RL load

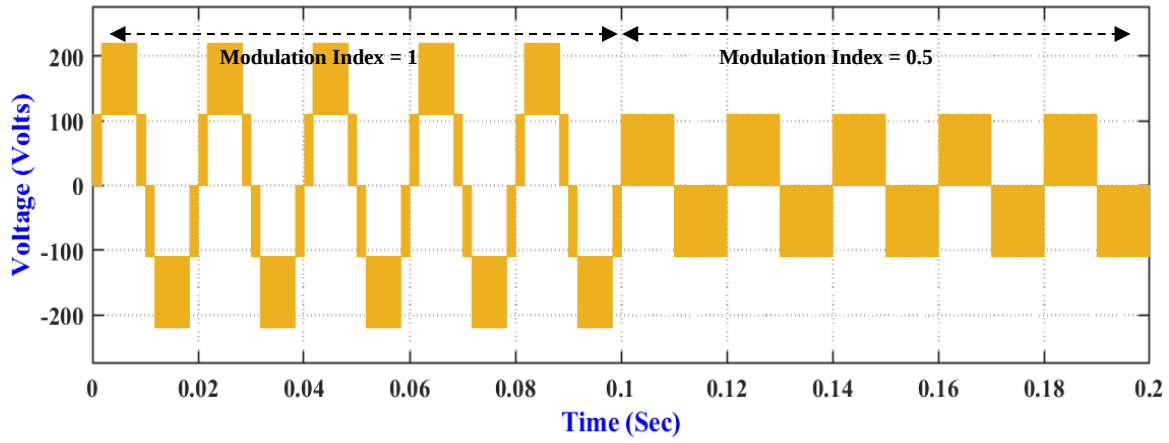

Figure 11. Output voltage with change in modulation index

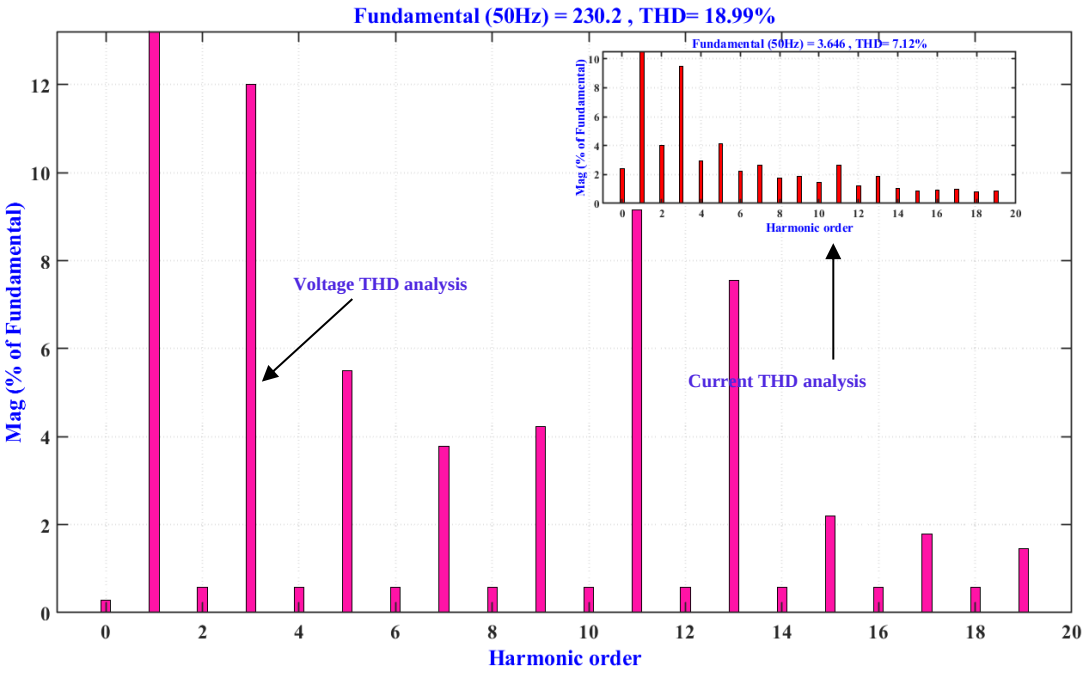

Figure 12. Voltage and current THD analysis for resistive load

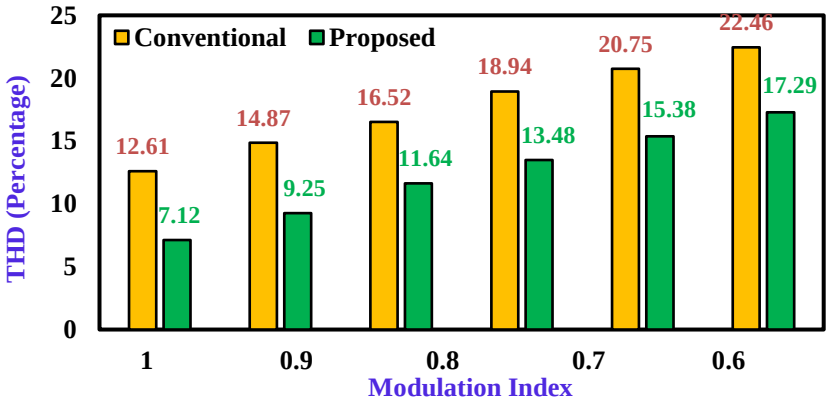

Figure 13. Current THD analysis for RL load

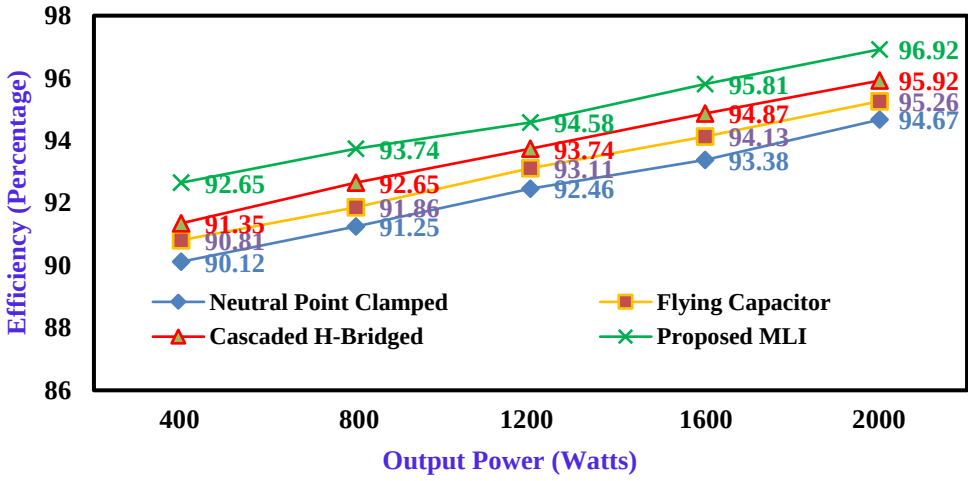

Figure 14. Efficiency analysis of proposed and conventional MLI

5. CONCLUSION

The proposed MLI's topology has been selected to enable the generating of multiple output levels, which led to output waveforms that are more identical and minimised voltage stress on the switches since there are fewer devices and switching losses. The inverter's performance has been assessed by simulating it under various operating conditions in terms of resistive and resistance with inductive load. The simulation findings unequivocally substantiated the superior performance of the five-level inverter over conventional counterparts, showcasing a notably lower THD of 7.12% and a marked enhancement in voltage output regulation. Moreover, the inverter exhibited an elevated power handling capacity, enabling it to efficiently manage higher power levels with an impressive efficiency rating of 96.92%. The five-level MLI offers considerable potential due to its ability to improve power conversion efficiency, reduce harmonic distortions, and integrate seamlessly with renewable energy sources.

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