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THD reduction in novel asymmetrical 21 level MLI using FLO-MOA algorithm optimized cascaded controller technique

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ABSTRACT

Since multi-level inverters (MLIs) may operate at lower switching frequencies and reduce switching losses, they are frequently used in high and medium electric drives for renewable energy applications. Lower-order harmonics could result from using a lower switching frequency, which would increase line current distortion. MLIs provide fewer output harmonics than traditional converters. This research suggested a hybrid strategy for creating a 21-level MLI. The suggested cascaded fractional-order tilt integral fractional-order proportional tilt derivative (FOTI-FOPTID) controller is used to adjust the switching pulse for the 21-level MLI. In this work, the Mother Optimization algorithm (MOA) is combined with the Frilled Lizard optimization (FLO) method to improve it. This results in the FLO-MOA algorithm, which is used to adjust the controller's gain parameters. This strategy reduces the number of switches and asymmetrical sources of dc voltage. The inverter's efficiency is raised, power loss is minimized, total harmonic distortion (THD) is decreased, and output voltage levels are improved.

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1. INTRODUCTION

Over the past few years, multi-level inverters (MLIs) have generally been utilized in great and medium power uses such as power conditioning, traction drives, high voltage direct current (HVDC), and power conditioning applications [1], [2]. MLIs are also referred to as electronic circuits, which are utilized for acquiring output voltages with the highest quality through the power switches of semiconductors [3], [4]. The MLIs have some advantages like reduction of harmonics, low electromagnetic interference, high efficiency, low-rated switches and higher quality waveforms [5], [6]. One of the important benefits of using MLI is the separation of DC sources. It is highly advantageous for the photovoltaic (PV) array and fuel cell applications. The MLI is categorized into three important configurations, and they are: flying capacitor clamped (FC) [7], neutral point clamped (NPC), or diode clamped [8], and cascaded H-bridge (CHB) inverters [9].

The major challenges of the conventional MLI configurations involve auxiliary components and switch quantity, which increases the inverter price and dimension. In FC and NPC MLI, the topologies are controlled by utilizing switching states [10]. The CHB inverters are utilized in medium and high voltage levels, while balancing the voltage is a complicated task in NPC and FC type inverters. Based on DC sources, CHB MLI are categorized into asymmetrical or symmetrical [11]. Despite the symmetrical topology's increased packing and similarity made possible by the H-bridge's shared structure, the total number of switches grows

exponentially with an upsurge in the output voltage. Increasing the output voltage level with few switches is possible in an asymmetric system. On the other hand, there are switches whose voltage ratings are nearly equivalent to the maximum voltage that can be used to increase the difficulty of the hardware circuit [12].

A decrease in efficiency is caused by an increase in switching and conduction loss as the total quantity of switches upsurges [13]. The growing quantity of switches has a number of drawbacks, including increased complexity, higher costs, and lower reliability [14]. The MLIs are implemented and designed using unsymmetrical DC sources for higher power application and grid integration to obtain high output voltage with a few number of switches. In existing works, some of the control approaches, such as modified SPWM and PWM are developed for getting the selective harmonic elimination (SHE). The switching stress is increased by using these techniques while the frequency is higher [15]. Jayakumar *et al.* [16] utilized the SHE method for investigating the asymmetric MLI with a reduced switch. Mohanty *et al.* [17] explained the low output voltage with reduced MLI utilizing the BWO algorithm. In the CHB MLIs, an improved artificial neural network (ANN) was utilized to minimize the total harmonic distortion (THD) [18]. Using a closed-loop controller, a five-level inverter is described in [19] for grid-connected PV applications that rely on switching capacitors. Improved grid-connected power quality is achieved by use of the CHB MLI by means of the NBO-RERNN method [20]. Despite the symmetrical topology's increased packing and similarity made possible by the H-bridge's shared structure, the total number of switches grows exponentially with an upsurge in the output voltage. However, some symmetric topologies aim to resolve this issue [21]. On the other hand, increasing output level with few switches is easily possible in an asymmetric system. This paper presents a 21-level MLI for reducing the THD utilizing a hybrid framework. The key objective of this paper is;

- To design a 21-level MLI that employs a hybrid technique aimed at minimizing THD.
- To tune the switching pulse of the 21-level MLI, the proposed cascaded fractional-order tilt integral fractional-order proportional tilt derivative (FOTI-FOPTID) controller is utilized.
- To augment the gain parameters of the controller, the FLO-MOA algorithm is proposed.

2. METHOD

MLIs have evolved dramatically due to high quality produce at a reduced cost. In the past few years, MLI has been used in the electronics and electrical market because of high voltage and high-power applications. However, the MLI faced high switching loss, high stress, low power, voltage balancing issues, driver circuit complexity, and high harmonics output distortion for medium voltage applications. A modern asymmetrical MLI with fewer switches needs to be introduced in this article. This article proposed a 21-level MLI design using the hybrid system for the reduction of total harmonics distortion and voltage stress in MLI. Here, PV is used to generate the maximum power to feed the input power to the MLI. Battery is utilized for storing the excess energy. The switching pulse of the 21 level MLI is tuned with the help of the proposed cascaded FOTI-FOPTID controller along with improved Frilled Lizard optimization (FLO) technique. The inspiration for FLO is the mechanism of position recognition and hunting strategy from the frilled lizard. In this work, the FLO algorithm is improved by integrating the Mother Optimization algorithm (MOA) with FLO. Thus, in this work FLO-MOA algorithm is proposed for tuning the gain parameters of the controller. This algorithm has high capability in exploration and exploitation, hence providing an efficient optimum solution. This algorithm will select the optimal gain parameter to reduce the THDs of the inverter and improve control. Figure 1 illustrates the block diagram for the recommended methodology.

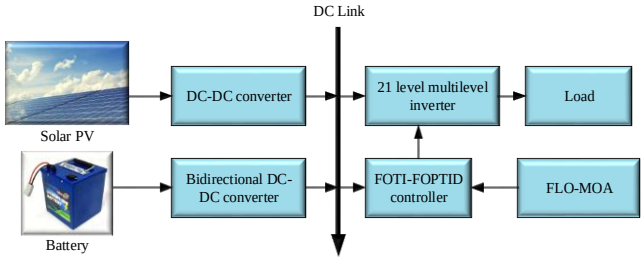


Figure 1. Graphical abstract

2.1. Modelling of solar photovoltaic

A PV cell typically contains a silicon-based P-N junction. When light strikes the cell, it frees electrons, which then travel through a closed electrical circuit. The PV module is a key component in solar power

generation, and its mathematical model is presented as [22], [23]. In this system, the circuit's output terminals are connected to load, and the voltage-current equation for the PV module is expressed as (1):

$$I = I_{PH} - I_0 \left[EXP\left(\frac{qV}{NKT}\right) - 1 \right] \quad (1)$$

From (1), the photo generated current for the solar cell is represented by I_{PH}, the reverse saturation current is indicated by I_0, the Boltzmann's constant is indicated by K, the temperature of the junction is denoted by T, the system's ideality factor is denoted by N, the charge of an electron and output voltage of the solar PV is specified by q and V. The series and parallel resistance of the solar PV are computed and articulated as (2) and (3);

$$I = I_{PH} - I_0 \left[EXP\left(\frac{qV}{NKT}\right) - 1 \right] - \frac{V+IR_S}{R_{SH}} \quad (2)$$

$$I = I_{PH} - I_0 \left[EXP\left(\frac{qV}{Nv_T}\right) - 1 \right] - \frac{V+IR_S}{R_{SH}} \quad (3)$$

The series and parallel resistance of the system are indicated by R_S and R_{SH}. A thermally generated voltage is indicated by v_T.

2.2. Modelling of battery

The state of charge (SoC) is vital in battery applications, and careful design is necessary to prevent challenges like undercharging, over-discharging, and overcharging. This paper adopts the ampere-hour counting method to compute the SoC [24], [25]. In this model, both the discharging or charging and the current value are measured and expressed as (4):

$$SoC = SoC_0 + \int_{\tau_0}^{\tau} \left(\frac{I_{BAT}}{C_{BAT}}\right) dt \quad (4)$$

The starting point of the battery SoC is represented by SoC_0, the time of starting point, and time of interest are indicated by τ_0 and τ. The battery current is represented as I_{BAT}, the battery capacity denoted by C_{BAT}. The losses involved in discharging, charging, and storing the battery are considered, and the SoC is determined and described as (5);

$$SoC = SoC_0 \left[1 - \frac{\mu}{24}(\tau - \tau_0)\right] + \int_{\tau_0}^{\tau} \left(\frac{I_{BAT}\eta_{BAT}}{C_{BAT}}\right) dt \quad (5)$$

From the above equation, the self-discharge rate is indicated by μ, the efficiency of battery discharging and charging is represented by η_{BAT}. The capacity of the battery is computed and expressed as (6);

$$C_{BAT} = C'_{BAT}\left(1 + \delta_C(T_{BAT} - 298.15)\right) \quad (6)$$

The battery's practical or available capacity is indicated as C_{BAT}, the nominal capacity of the battery is represented by C'_{BAT}. Thus, the current of the battery is computed as (7):

$$I_{BAT} = \frac{P_{SOLAR} + P_{WIND}\mu_{RECTI} - P_{Load}/\mu_{INVER}}{V_{BAT}} \quad (7)$$

From (7), the power of the load, wind turbine, and PV solar is indicated by P_{Load}, P_{WIND}, and P_{SOLAR}. The voltage of the battery is denoted by V_{BAT}.

2.3. Proposed 21 level multi-level inverter

A novel 21-level MLI is suggested with a reduced quantity of switches, as shown in Figure 2. The proposed 21-level MLI configuration consists of 8 controlled switches and employs three asymmetric DC sources deprived of requiring any diodes, inductors or capacitors. Several power quality issues, including cost, cost per unit based on multiple weight factors, THD, voltage stress, component count, switch count, and MLI topology, are minimized. The voltage magnitude, Vdc, is determined using a trinary proportion of 1:3:6 to generate a 21-level output voltage. Additionally, employing source voltage for output voltage generation can lead to reduced voltage stress on components and improved efficiency [26]. The value of asymmetrical dc voltage sources are 1 V, 3 V, and 6 V respectively.

In order to preserve the intended dc-link voltage ratio of 1:3:6, the inverter module gets input from three asymmetrical voltage sources via separate DC rectifying circuits. Based on a step voltage of Vdc, this configuration makes it possible to generate 21 voltage levels, including ±10Vdc, ±2Vdc, ±Vdc, and 0. Greater voltage for some switches and greater costs for switches and DC sources will result from a larger number of DC sources and their

lower utilization. This consideration of these problems focuses on the many switching states and modes of operation of the 21-level inverter [27]. Figure 2 illustrates the circuit figure of the suggested 21 level MLI.

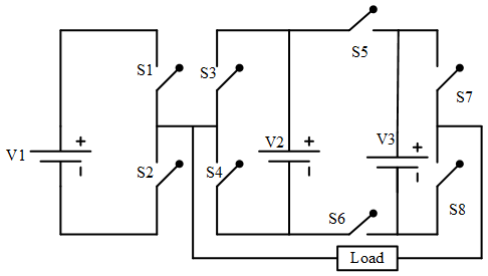


Figure 2. Circuit diagram of suggested 21 level MLI

In mode 1, the switches S1, S4, S6, and S8 turn on and the dc sources will not get acted or conducted. In mode 2, the switches S2, S4, S6, and S8 turn on, and the positive polarity of dc source V1 only gets conducted or acted. In mode 3, switches S1, S4, S5, and S7 are activated, allowing V2 to conduct. In mode 4, V3 conducts due to the activation of switches S1, S3, S5, and S8. In mode 5, switches S1, S4, S5, and S8 are turned on, resulting in the action of the dc sources V2 and V3 (V2+V3). Finally, in mode 6, switches S2, S4, S5, and S8 are activated, allowing the dc sources (V1+V2+V3) to conduct. Figure 3 depicts the methods of operation; (a) mode 1 (0V), (b) mode 2 (V1), (c) mode 3 (V2), (d) mode 4 (V3), (e) mode 5 (V2+V3), and (f) mode 6 (V1+V2+V3). Table 1 depicts the switching states.

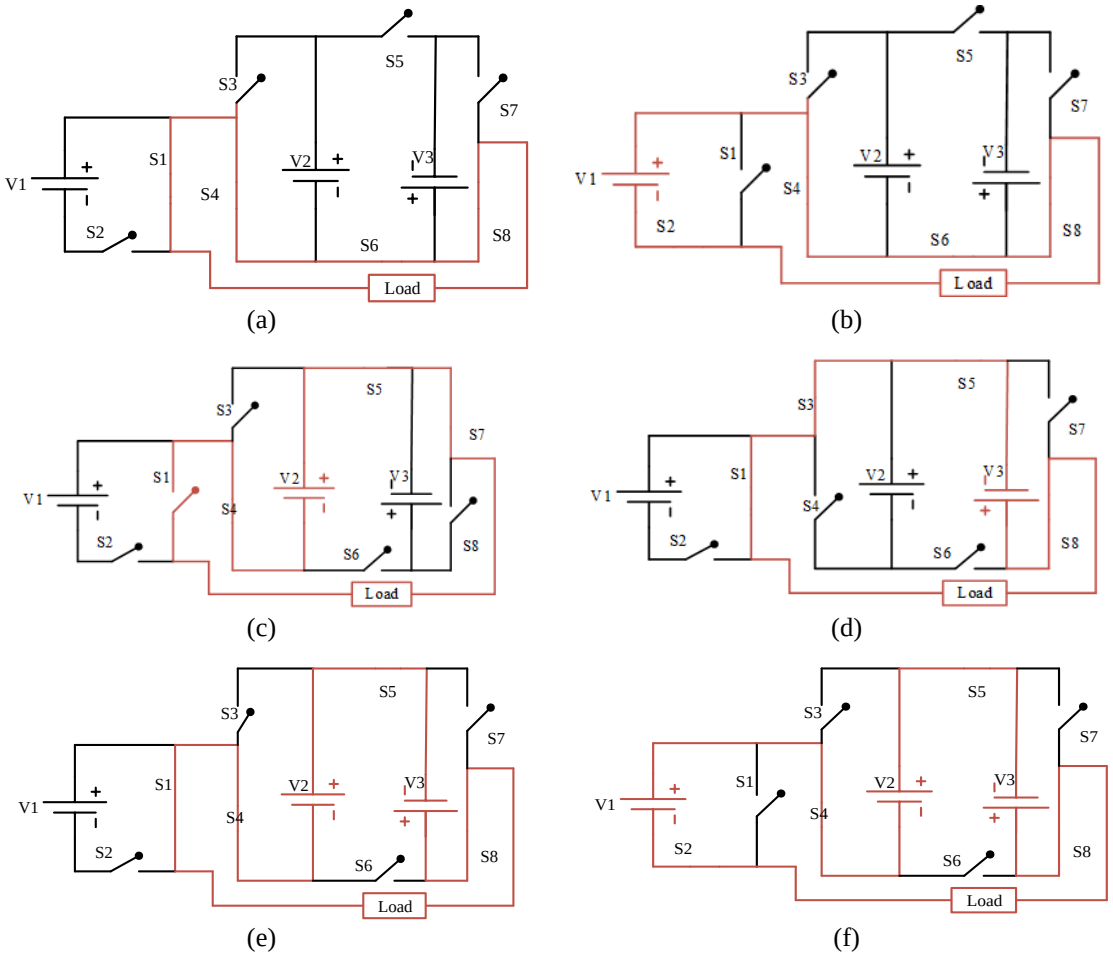


Figure 3. Modes of operation; (a) mode 1 (0V), (b) mode 2 (V1), (c) mode 3 (V2), (d) mode 4 (V3), (e) mode 5 (V2+V3), and (f) mode 6 (V1+V2+V3)

Table 1. Switching states

Vdc	S1	S2	S3	S4	S5	S6	S7	S8
+10 Vdc	0	1	0	1	1	0	0	1
+9 Vdc	1	0	0	1	1	0	0	1
+8 Vdc	1	0	1	0	1	0	0	1
+7 Vdc	1	0	0	1	0	1	1	0
+6 Vdc	1	0	1	0	1	0	0	1
+5 Vdc	1	0	0	1	0	1	0	1
+4 Vdc	0	1	0	1	1	0	1	0
+3 Vdc	1	0	0	1	1	0	1	0
+2 Vdc	1	0	0	1	1	0	0	1
+1 Vdc	0	1	0	1	0	1	0	1
0	1	0	0	1	0	1	0	1
-1 Vdc	1	0	1	0	1	0	1	0
-2 Vdc	1	0	1	0	0	1	0	0
-3 Vdc	0	1	1	0	0	1	0	1
-4 Vdc	1	0	1	0	0	1	0	0
-5 Vdc	0	1	0	0	1	0	1	0
-6 Vdc	0	1	0	1	0	1	1	0
-7 Vdc	0	1	0	0	1	0	1	0
-8 Vdc	0	1	0	0	0	1	0	1
-9 Vdc	1	1	1	0	0	1	1	0
-10 Vdc	0	1	1	0	0	1	1	0

2.4. FOTI-FOPTID controller

A fractional-order operator indicates the functionality of either a fractional-order integrator or differentiator. Dynamic controllers or systems can include fractional-order operators. System modeling and controller design are made possible by adding two more degrees of freedom from these fractional orders [28].

The FOTI controller has a similar structure to the FOPI controller, with both featuring a fractional-order (or non-integer) integrator. However, in the FOTI design, the proportional component is replaced by a tilt controller. The FOTI controller combines the characteristics of both TID and FOPID controllers, enabling it to achieve better performance and improved robustness. The FOTI controller's transfer function is calculated and expressed as (8);

$$G_{FOTI}(S) = \frac{K_{t_1}}{\frac{1}{S^{N_1}}} + \frac{K_{I_1}}{S^{\mu_1}} \tag{8}$$

From (8), the tilted gain and integral gain for the FOTI controller are represented by K_{t_1} and K_{I_1}. The non-zero tilt parameter of the FOTI controller is represented by N_1. The fractional-order of the FOTI controller is denoted by μ_1. The FOPTID controller combines the benefits of both TID and FOPID controllers. Therefore, a hybrid controller can enhance system response by providing increased robustness, flexibility, and an improved ability to reject disturbances. This is how the FOPTID controller's transfer function is written;

$$G_{FOPTID}(S) = \frac{U(S)}{E(S)} = K_P + \frac{K_{t_2}}{\frac{1}{S^{N_2}}} + \frac{K_{I_2}}{S^{\mu_2}} + K_D S^{\beta} \tag{9}$$

From (9), the tilted gain and integral gain for the FOPTID controller are represented by K_{t_2} and K_{I_2}. The fractional-order of the FOPTID controller is denoted by μ_2. The proportional gain of the FOPTID controller is indicated by K_P. The fractional-order of the tilt action and the derivative gain is denoted by N_2 and K_D. The fractional order operator of the differential terms is indicated by β.

The equation reveals that the FOPTID controller has seven parameters $(K_P, K_t, N, K_I, \mu_2, K_D, \beta)$ that need to be optimized. The FOPTID controller provides more versatility than both the TID and FOPID controllers [29]. The suggested hybrid FOTI-FOPTID controller's transfer function is calculated and given as;

$$G_{FOTI-FOPTID}(S) = \frac{K_{t_1}}{\frac{1}{S^{N_1}}} + \frac{K_{I_1}}{S^{\mu_1}} + K_P + \frac{K_{t_2}}{\frac{1}{S^{N_2}}} + \frac{K_{I_2}}{S^{\mu_2}} + K_D S^{\vartheta} \tag{10}$$

Figure 4 elucidates the structure of the FOTI-FOPTID controller.

2.5. Hybrid Frilled Lizard optimization-mother optimization algorithm

In this section, a new mixture metaheuristic algorithm trusts the strength of the FLO algorithm and MOA to tune the gain parameters of the controller. A new hybrid FLO-MOA is proposed to leakage local optima while also attractive both the speed of convergence and the level of accuracy. The FLO's exploration

capabilities are enhanced by incorporating the MOA's exploration elements. The modifications in the MOA's structure boost its exploration capabilities by integrating the exploitation features from the FLO, thus establishing a balance between exploration and exploitation.

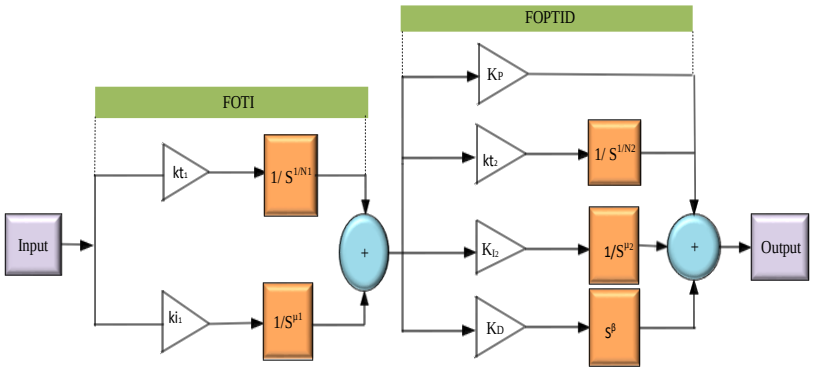


Figure 4. Block diagram of FOTI-FOPTID controller

2.5.1. Frilled Lizard optimization algorithm

The frilled lizard goes to eat and then climbs to the top of a close tree [30]. The algorithm's capacity to successfully utilize local search is enhanced by simulating this movement, which leads to little changes in the population's placements inside the solution space. During the FLO phase, each person in the population has their place changed based on the frilled lizard's strategy for getting back to the top of the tree after eating.

A computer model of the frilled lizard climbing a nearby tree is used to find a new spot for each member of the population. This model is based on (11). If the new position raises the objective function value, it takes the place of the person's old position, as shown in (12).

$$y_{j,e}^{P2} = y_{j,e} + (1-2\gamma).\frac{(UB_e - LB_e)}{t}, j = 1,2,\ldots\ldots,N, e = 1,2,\ldots.,Mandt = 1,2,\ldots.,T \quad (11)$$

$$Y_{j1} = \begin{cases} Y_j^{P2}, F_j^{P2} < F_j \\ Y_j, else \end{cases} \quad (12)$$

From (11) and (12), the new position for the candidate solution is denoted by Y_j^{P2}, the value of the objective function is denoted by F_j^{P2}, the algorithm's iteration counter is denoted by τ, the maximal number of iterations is denoted by T, and the FLO's e^{th} dimension is denoted by $y_{j,e}^{P2}$.

2.5.2. Mother optimization algorithm

The initial phase of population updating in the MOA, known as "Education," is modeled after the process of educating children [31]. The objective is to enhance exploration abilities and global search by making substantial changes to the positions of the populace members. In the MOA algorithm, the mother is regarded as the highest-performing individual within the population. The role of guiding the offspring is modeled to reflect the process of education within the algorithm's framework. As shown in (13) is used to determine each person's new position. According to (14), the person will be in a new place if the new location makes the objective function value better.

$$y_{j,k}^{P1} = y_{j,k} + R(0,1).\left(mother_k - R(2).y_{j,k}\right) \quad (13)$$

$$Y_{j2} = \begin{cases} Y_j^{P1}, F_j^{P1} \leq F_j \\ Y_j, else \end{cases} \quad (14)$$

From (13) and (14), the mother's position in k^{th} dimension is represented by $mother_k$, k^{th} dimension of j^{th} population member Y_j is denoted by $y_{j,k}$, the new position of j^{th} population member is denoted by y_j^{P1}, and k^{th} dimension is represented by $y_{j,k}^{P1}$, the objective function value is characterized by F_j^{P1}, the random number between the interval of 0 and 1 is indicated by $R(0,1)$ as well as the $R(2)$ function generates a arbitrary amount uniformly from the regular {1, 2}. Figure 5 illustrates the flowchart of FLO-MOA.

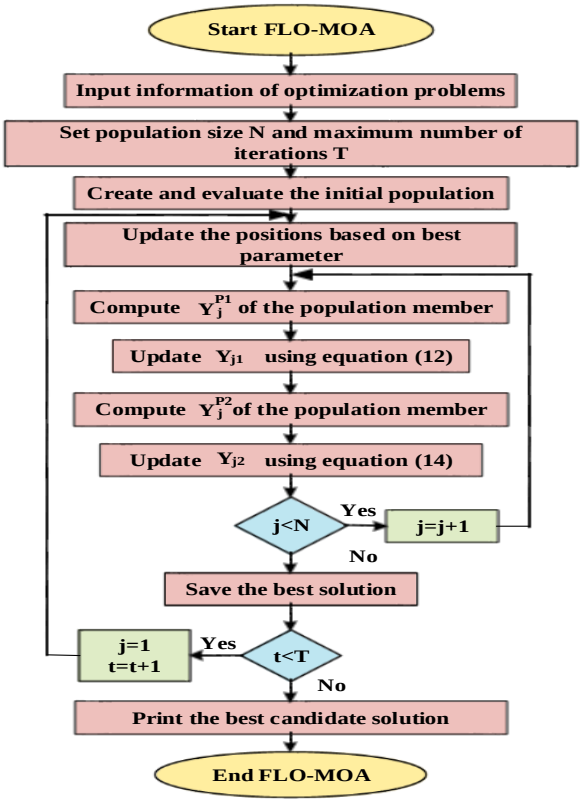


Figure 5. Flowchart of FLO-MOA

3. RESULTS AND DISCUSSION

The proposed hybrid FLO-MOA algorithm has been implemented in MATLAB to obtain optimized switching angles while minimizing switch MLI. Simulink has been used to simulate the MLI. By employing equal voltage sources, multiple voltage levels have been generated. For validation, the effectiveness of the FLO-MOA algorithm has been illustrated through its implementation in the MATLAB/Simulink environment. Figure 6 depicts the Simulink block for the proposed methodology. Table 2 illustrates the system parameters.

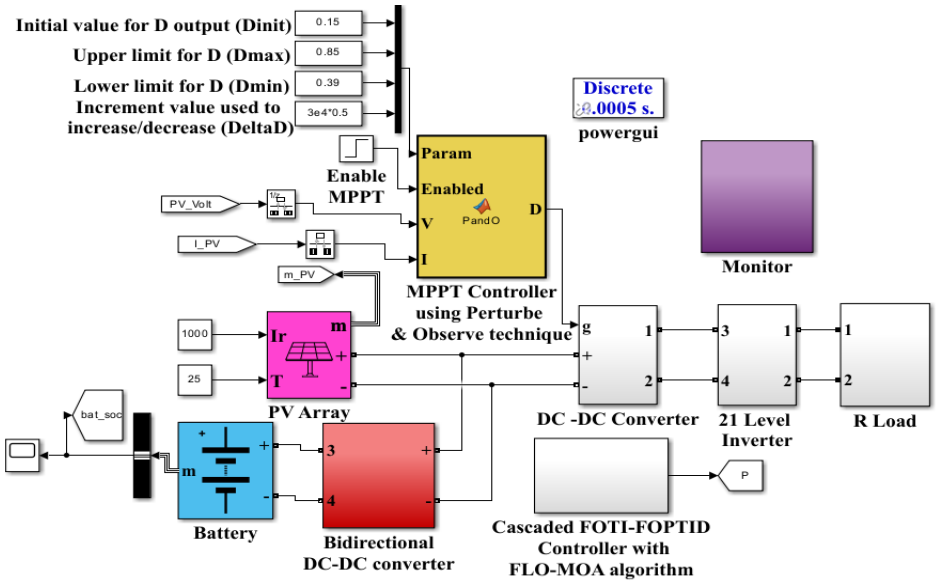


Figure 6. Simulink block for the proposed methodology

Table 2. System parameters

Parameter	Values
Maximum power	305.226 W
Open circuit voltage	64.2 V
Short circuit current	5.96 A
Voltage at maximum power point	54.7 V
Diode ideality factor	0.94489
Shunt resistance	393.20 Ω
Series resistance	0.37428 Ω
Nominal voltage	200 V
Rated capacity	Ah
Battery response time	1 s

The PV system's input and output characteristics are displayed in Figure 7. The PV system's inputs are temperature and solar irradiation, which are both fixed at 25 °C and 1000 W/m^2, respectively. The PV voltage and current rise in these circumstances. Additionally, the diode current also increases as the PV output rises. This behaviour reflects the typical response of the PV system to stable input conditions.

Figure 8 depicts the output of the dc link. The outputs of solar PV and battery are given to the dc link. The dc voltage rises rapidly from 0 V to about 300 V, then falls a bit before levelling off around that value. The dc link voltage dips due to following reasons, power drawn by the inverter is greater than power supplied by PV and battery (or supply is delayed), so the dc link capacitor discharges. Similarly, the dc increases from 0 A to nearly 20 A and then remains at that level. The dc power shows a similar trend, quickly increasing to around 6000 W before becoming stable.

Figure 9 provides the output of the battery. In this figure, SoC begins at 50% and slightly drops to about 49.98%, indicating energy consumption. The current remains stable at approximately 20 A throughout the duration. Meanwhile, the voltage starts at around 212 V and gradually decreases.

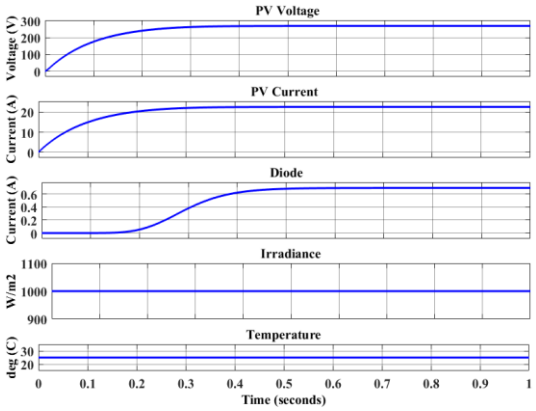


Figure 7. PV input and output characteristics

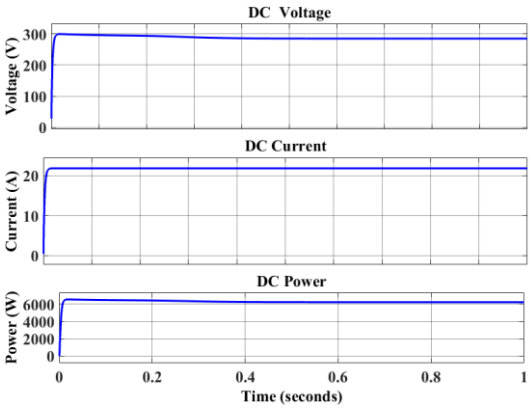


Figure 8. DC link output

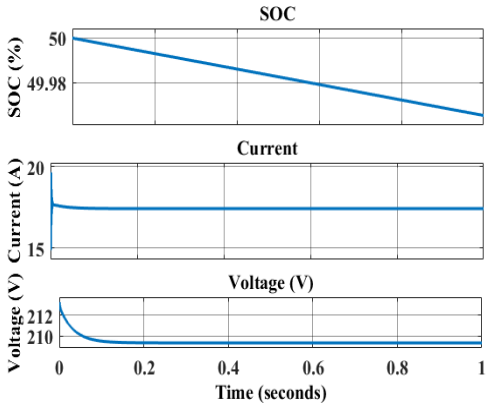
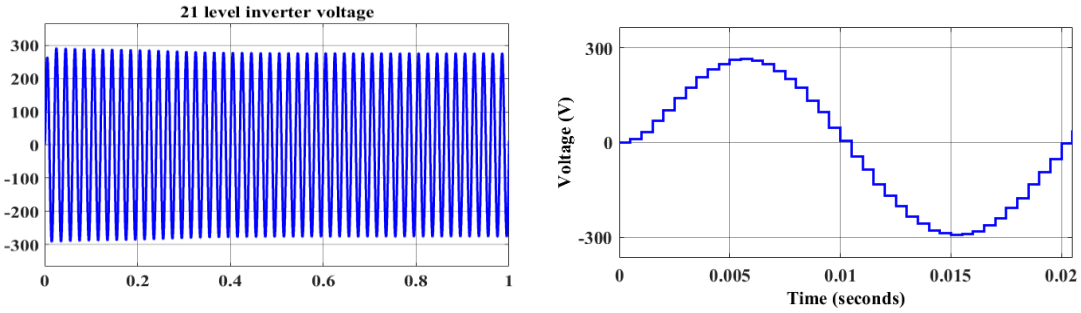


Figure 9. Battery outputs

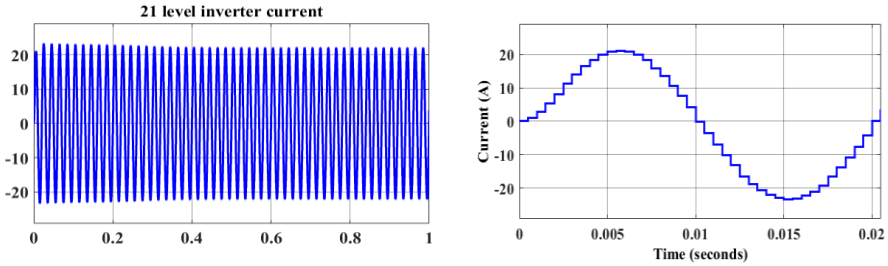
Figures 10(a) and (b) illustrates the output voltage waveform for the proposed 21-level hybrid MLI system. The resultant output voltage is smooth and closely approximates a sinusoidal waveform. The augmented number of output steps leads to a decrease in the THD related to the output voltage.

Figures 11(a) and (b) depicts the output current waveform for the suggested 21-level hybrid MLI topology. The inverter current waveform is a stepped waveform with 21 distinct levels, allowing the current to assume 21 different discrete values. This waveform is symmetrical, exhibiting positive and negative peaks of equal magnitude.



(a) (b)

Figure 10. Inverter voltage; (a) switching high frequency voltage waveform and (b) zoomed staircase approximation of a sinusoidal cycle of 21 level



(a) (b)

Figure 11. Inverter current; (a) switching high frequency current waveform and (b) zoomed staircase approximation of a sinusoidal cycle of 21 level

Figure 12 illustrates the 21-level output voltage waveform's FFT analysis. According to the procedure for determining the number of steps in the output voltage waveform, the output should consist of 21 steps, as illustrated in the image. This high step count allows the waveform to closely resemble a sinusoidal shape, resulting in a minimal THD of just 1.11%.

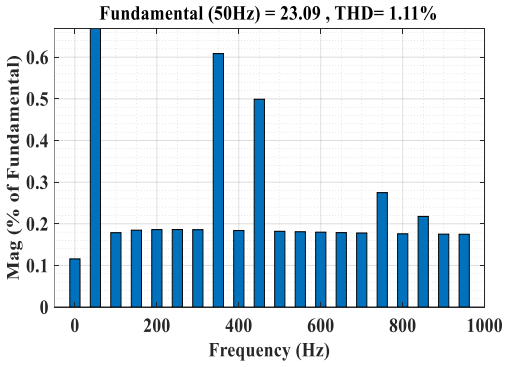
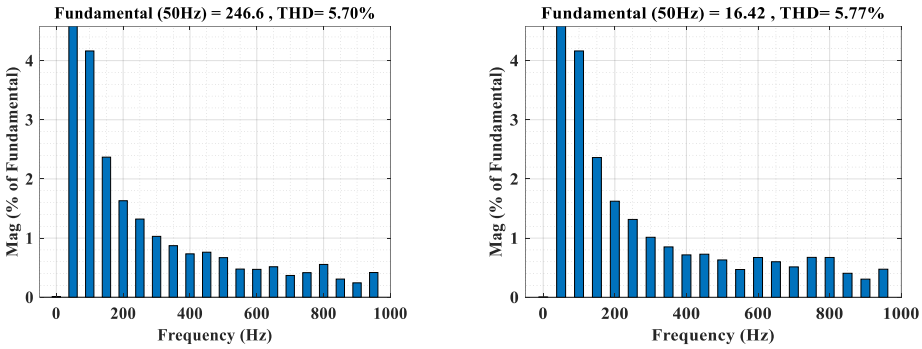


Figure 12. FFT analysis for proposed controller

Figures 13(a) and (b) presents the THD analysis for voltage and current in a system without a controller. Without controller, the THD voltage is 5.70%, and the THD current is 5.77%. These values indicate a higher level of harmonic distortion in both voltage and current compared to the system with a controller. The results emphasize the importance of using a controller to reduce THD levels, thereby improving power quality.

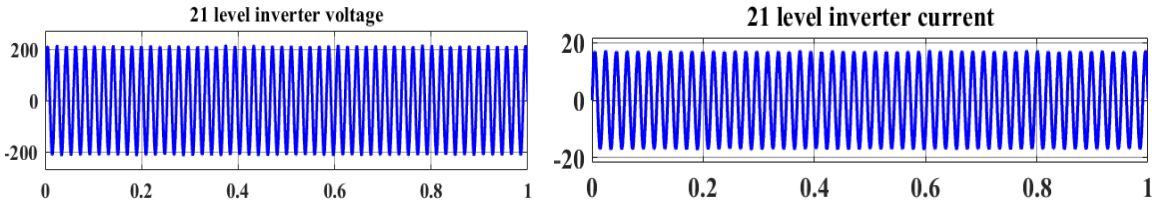


(a) (b)

Figure 13 Analysis of THD; (a) THD voltage without controller and (b) THD current without controller

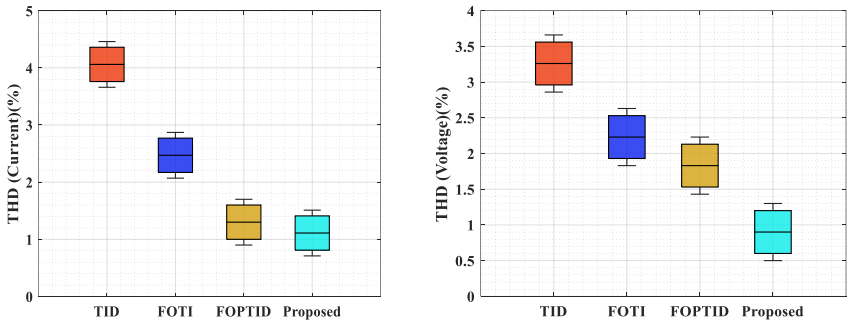
Figures 14(a) and (b) shows the analysis of inverter voltage and current without a controller. The voltage waveform of the 21-level inverter is a smooth, sinusoidal signal with a peak-to-peak amplitude of around 400 V. In contrast, the current waveform is similarly smooth, with an amplitude of about 40 A. This multi-level topology likely enhances the quality of both output voltage and current by achieving a high quantity of voltage levels.

Figures 15(a) and (b) illustrates the THD analysis for current and voltage. The box plot compares the THD of different configurations. The proposed exhibits the lowest median THD, indicating its superior performance in reducing harmonic distortion. On the other hand, TID exhibits the highest THD. FOTI and FOPTID configurations show intermediate THD levels.



(a) (b)

Figure 14. Inverter output waveforms; (a) inverter voltage without controller and (b) inverter current without controllers



(a) (b)

Figure 15. THD comparison; (a) THD value of current for different controllers and (b) THD value of voltage for different controllers

Figure 16 illustrates the relative investigation of swapping devices. The proposed topology offers fewer switching devices compared to other designs in the comparison. This reduction minimizes the losses typically associated with these switches. As a result, the system experiences lower energy dissipation. This contributes to an increase in overall efficiency.

Figure 17 depicts the comparative analysis of voltage sources. The graph illustrates the quantity of voltage sources used in existing studies [26], [27], [29], [30], and the proposed method). The Y-axis represents the number of voltage sources, ranging from 0 to 6. Among the systems, [27] uses the highest number (5), while [26], [29], [30] each use 4 voltage sources. The proposed method stands out with the least, using only 3. This indicates that the suggested approach is more resource-efficient in terms of voltage sources compared to the others.

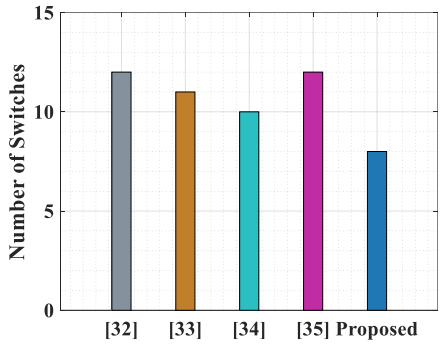


Figure 16. Comparative analysis of switching devices

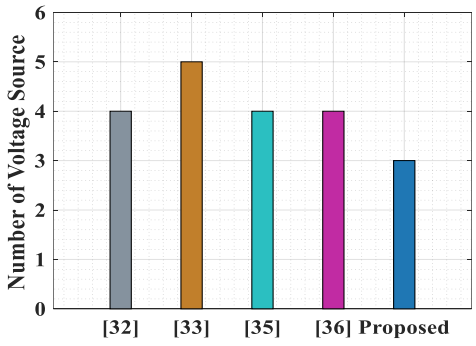


Figure 17. Comparative analysis of voltage sources

Figure 18 shows the study of efficiency. The suggested controller has a higher efficiency of 98.19%. The existing FOPTID, FOTI, and TID controllers have low efficiency of 97.27%, 96.72%, and 95.01%. When compared to other existing controllers, the proposed controller has high efficiency.

Figure 19 illustrates the total power loss in watts (W) across four different control strategies: TID, FOTI, FOPTID, and the proposed method. The TID strategy exhibits the highest power loss, indicating a significant inefficiency. When compared to TID, the FOTI approach exhibits a moderate reduction in power loss; however, the FOPTID strategy substantially reduces the loss, indicating increased efficiency. The proposed method results in a minimal power loss of 17.58 W, highlighting its effectiveness in optimizing performance.

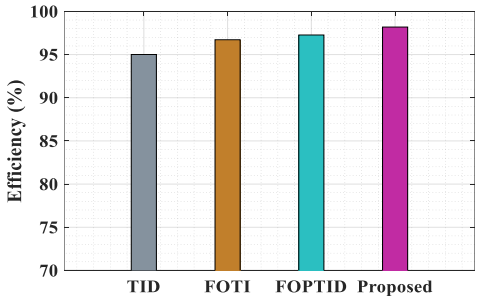


Figure 18. Analysis of efficiency

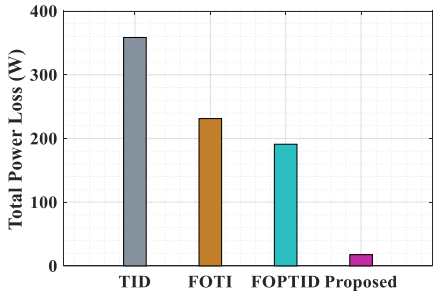


Figure 19. Analysis of power loss

Figure 20 depicts the convergence plot of the proposed FLO-MOA, where MOA represents the Mother Optimization algorithm, PSO stands for particle swarm optimization, FLO denotes the Frilled Lizard optimization, and GA denotes the genetic algorithm. The proposed algorithm showed a minimum fitness is acquired by the 16th iteration. Existing optimizations like PSO, MOA, FLO, and GA require more iterations of 44, 46, 77, and 79, respectively.

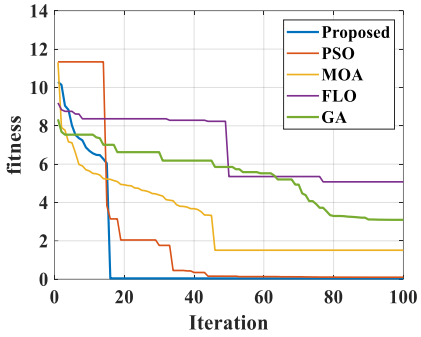


Figure 20. Convergence plot

4. CONCLUSION

The proposed novel asymmetrical 21-level MLI integrated with the FLO–MOA algorithm optimized cascaded FOTI–FOPTID controller has demonstrated significant potential in reducing THD compared to conventional optimization and control strategies. The hybrid use of FLO and MOA has ensured better exploration–exploitation balance, achieving optimal switching angles and control parameters for harmonic minimization. Simulation and analysis confirm that the developed technique enhances output voltage quality, reduces switching losses, and improves dynamic stability, making it suitable for renewable energy integration, electric vehicle drives, and power quality improvement applications. While this study has demonstrated significant success, several avenues remain open for further investigation and enhancement of the proposed system. To further advance this research, the following directions are recommended: real-time hardware implementation, hybrid energy systems, AI-enabled controllers, real-time optimization, renewable energy applications and adaptive and self-tuning control.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author, [initials: MDR], upon reasonable request.

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