High-performance voltage control of ladder boost converters using robust backstepping sliding mode control

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Article Info

Article history:

Received Jul 18, 2025
Revised Jan 5, 2026
Accepted Feb 22, 2026

Keywords:

Backstepping sliding mode control
High-gain DC-DC converter
Ladder boost converter
Output voltage regulation
Renewable energy integration
Robust nonlinear control

ABSTRACT

This paper presents a control-focused solution for high-gain DC-DC conversion by integrating a capacitor-diode ladder boost converter (CDLBC) with a backstepping sliding mode control (BSMC) scheme. While the CDLBC topology provides modular voltage gain at moderate duty ratios, the core contribution lies in the development of a robust control strategy to address the converter's nonlinear and multistage dynamics. The proposed BSMC method combines the recursive design of backstepping with the finite-time convergence and disturbance rejection properties of sliding mode control (SMC). A saturation function is employed to suppress chattering and ensure smooth control action. The controller is derived based on Lyapunov stability theory and implemented on a digital signal processor without requiring hardware modification. Experimental results under various output voltage transitions show that the BSMC approach significantly improves transient performance, reduces voltage ripple, and enhances regulation accuracy compared to conventional SMC. These findings confirm the effectiveness and practicality of software-based robust control for efficient and adaptive DC-DC power conversion in renewable energy and embedded applications.

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1. INTRODUCTION

The escalating demand for clean energy solutions and the global urgency to transition away from fossil fuel dependency have catalyzed widespread adoption of renewable energy technologies [1]-[3]. Photovoltaic (PV) arrays, hydrogen fuel cells, and wind energy systems are becoming central elements in both off-grid and grid-connected infrastructures [4], [5]. This paradigm shift is further accelerated by the electrification of transportation, the proliferation of residential solar installations, and the increasing emphasis on energy decentralization [6]. Despite these advances, renewable sources inherently suffer from two critical drawbacks: low and fluctuating output voltages, and susceptibility to environmental variability. These characteristics present significant challenges for conventional power processing systems and necessitate the development of efficient, flexible, and dynamically responsive DC-DC conversion architectures [7]-[10].

Among the fundamental converter topologies, the classical boost converter remains a prevalent solution for stepping up low input voltages from renewable energy sources such as PV panels and fuel cells [11]. Its structural simplicity, reliance on a single active switch, and ease of control implementation have made it a default choice in low-to-medium power applications [12]. However, when high voltage gain is required, especially under fast-changing operating conditions or load variations, the classical boost converter reveals several critical limitations. Most notably, the voltage gain increases nonlinearly as the duty ratio approaches unity, leading to severe efficiency degradation due to elevated conduction and switching losses [13]. At high duty cycles, the converter also subjects the inductor and switch to substantial current stress, which accelerates thermal aging and reduces overall system lifespan [14].

Additionally, from a control standpoint, the classical boost converter exhibits non-minimum phase behavior due to the presence of a right-half-plane zero in its control-to-output transfer function. This inherent characteristic restricts the bandwidth of linear control schemes and compromises dynamic response [15]. During large signal transients or in the presence of load disturbances, the converter struggles to maintain output stability, resulting in overshoots, slow settling, and oscillatory behavior [16]. Furthermore, conventional implementations heavily rely on hardware-centric configurations. When adapting to new output voltage levels or modified load requirements, these designs often require circuit redesign or component replacement [17]. Such rigidity increases development time and cost while reducing the flexibility of the system. This limitation is particularly challenging in modern applications that demand compact size, scalability, and rapid deployment in fields such as renewable energy integration, electric mobility, and embedded power systems [18], [19].

In parallel with hardware advancements, modern control theory has introduced powerful tools to enhance both dynamic regulation and robustness against external disturbances and internal uncertainties. Among these, sliding mode control (SMC) has gained prominence due to its inherent robustness against parameter variations and load perturbations, as well as its finite-time convergence properties [20], [21]. Similarly, adaptive control and model reference adaptive control strategies have demonstrated the ability to maintain system stability in the face of uncertain or time-varying plant dynamics [22]. In addition, bio-inspired and soft computing approaches, including fuzzy logic control, neural networks, and genetic algorithms, have enabled adaptive tuning and nonlinear approximation in complex systems [23]. These intelligent methods offer promising performance in modeling uncertainties and enhancing control flexibility. However, their practical deployment, particularly in real-time embedded applications, may face challenges related to computational burden, training data quality, and system integration [24].

As a result, there is increasing interest in hybrid control strategies that combine the interpretability and structural simplicity of classical methods with the robustness of nonlinear and intelligent approaches [25]. Among such methods, backstepping sliding mode control (BSMC) emerges as a compelling candidate. By integrating the recursive design process of backstepping with the disturbance rejection capabilities of sliding mode theory, BSMC enables effective controller synthesis for higher-order nonlinear systems without requiring model linearization [26]. It has found successful applications in areas such as motor drives and grid-connected power converters due to its adaptability and real-time feasibility [27]. Given these strengths, BSMC is particularly well-suited for controlling DC-DC converters, where accurate, reliable, and efficient voltage regulation is essential under varying operating conditions.

To overcome the limitations of classical boost converters, such as low efficiency at high duty cycles, limited flexibility, and poor transient response, this study develops a capacitor-diode ladder boost converter (CDLBC) integrated with a robust BSMC strategy. The proposed CDLBC achieves significant voltage amplification while maintaining a low input voltage, supporting compact and efficient implementations for PV and portable applications. The BSMC scheme is specifically designed to regulate the CDLBC output under varying operating conditions without hardware modification. Experimental validation confirms the proposed method's effectiveness, demonstrating improved steady-state accuracy and dynamic performance compared to conventional SMC. This work represents the first experimental application of BSMC tailored to the CDLBC architecture.

2. PROBLEM STATEMENT OF CONVENTIONAL STEP-UP CONVERTERS

The classical boost converter is a fundamental topology widely used in low-to-medium power applications to step up voltage levels from energy sources such as PV panels, batteries, or fuel cells. The topology comprises a single inductor, a power switch, a diode, and an output capacitor. Its popularity stems from its structural simplicity, compactness, and ease of control implementation. However, as modern applications demand higher voltage gain, improved efficiency, and enhanced dynamic performance, the inherent limitations of this traditional converter have become increasingly apparent.

In continuous conduction mode (CCM), assuming ideal components, the steady-state voltage gain is expressed as (1):

$$\frac{v_o}{v_{in}} = \frac{1}{1-D} \tag{1}$$

where v_o is the output voltage, v_{in} is the input voltage, and $D \in (0,1)$ is the duty ratio of the switch. As D approaches unity, the gain increases significantly. However, high duty ratios induce considerable current stress, increased switching losses, and reduced efficiency due to non-ideal effects such as diode voltage drops and parasitic resistances.

From a dynamical perspective, the classical boost converter exhibits a right-half-plane zero in its control-to-output transfer function, making it a non-minimum phase system. This characteristic inherently limits the achievable control bandwidth and degrades the transient response. The averaged state-space model under CCM operation is given by (2) and (3):

$$L\frac{di_L}{dt} = v_{in} - Dv_o \tag{2}$$

$$C\frac{dv_o}{dt} = Di_L - \frac{v_o}{R} \tag{3}$$

where i_L is the inductor current, L and C are the inductance and output capacitance, respectively, and R is the resistive load. These nonlinear coupled equations highlight the difficulty of achieving precise regulation with linear controllers under varying conditions. As the demand for high voltage gain continues to rise in applications such as electric vehicles, grid-connected PV systems, and telecommunication power supplies, conventional boost converters face major drawbacks when operated at extreme duty ratios. These include excessive stress on power components, degraded efficiency, and limited control performance.

Remark 1: the classical boost converter, though simple and widely adopted, suffers from critical intrinsic drawbacks under high-gain operation. These include severe efficiency loss, restricted dynamic bandwidth due to RHP zero, and high sensitivity to disturbances. Such limitations make it unsuitable for applications requiring both compact hardware and robust, responsive control. To overcome these limitations while maintaining simplicity and transformer less design, multistage and ladder-based architectures have gained considerable attention. Among them, the CDLBC has emerged as a promising candidate, offering high voltage gain and modular scalability. The following section details its structure and operational principles.

3. HIGH-GAIN BOOST CONVERTER AND NONLINEAR CONTROL STRATEGY

The capacitor-diode ladder boost converter is designed to address the gain limitations and efficiency issues of conventional boost converters. It achieves higher voltage conversion ratios by cascading multiple capacitor-diode cells in a ladder configuration, operating under a single active switch and driven by a standard pulse width modulation (PWM) signal. Each stage of the ladder consists of a diode-capacitor pair. When properly timed, the charging and discharging of the capacitors result in a voltage stacking effect, enabling the converter to reach output voltages significantly higher than the input without requiring excessively high duty ratios. The output voltage of a k-stage CDLBC can be approximately expressed as (4):

$$v_o = \frac{v_{\text{in}}}{1-D} \cdot (k+1) \tag{4}$$

where v_o is the output voltage, v_{in} is the input voltage, D is the switching duty ratio, and k denotes the number of capacitors–diode stages. This relationship highlights the advantage of the CDLBC in achieving high voltage gain at moderate duty cycles, thereby reducing switching losses and improving converter efficiency.

Remark 2: the CDLBC offers a transformer less and modular approach to achieving high voltage gain at moderate duty cycles. Its structure eliminates the need for magnetic components, thereby reducing weight, cost, and electromagnetic interference while improving energy density. This makes it especially attractive for space-constrained, high-efficiency applications such as PV systems and portable electronic devices. However, the multistage nature of the CDLBC also introduces internal complexity and potential voltage imbalance, necessitating the integration of robust and intelligent control strategies.

Despite these benefits, the CDLBC introduces more complex internal dynamics due to the multiple interacting capacitors and diodes. Voltage imbalance, component mismatch, and transient overshoot are potential concerns that must be addressed through robust control schemes. Therefore, the integration of a dynamic control strategy becomes crucial to maintain output voltage regulation in the presence of input disturbances, load variation, and component nonlinearities. To address these challenges, a hybrid control approach that combines backstepping and sliding mode principles is proposed to enhance the dynamic performance and robustness of the CDLBC. The structural configuration of the proposed CDLBC and its overall control strategy using the BSMC approach are depicted in Figure 1, providing the basis for the subsequent modeling and controller design. Let v_o denote the output voltage, i_L the inductor current, and v_{ref} the voltage reference. Define the tracking error:

$$e_1 = v_o - v_{ref} \tag{5}$$

A virtual control input $\alpha(i_L)$ is introduced via backstepping to stabilize v_o. The Lyapunov function candidate is (6):

$$V_1 = \frac{1}{2} e_1^2 \tag{6}$$

Differentiating V_1 and substituting the output dynamics yields (7):

$$\dot{V}_1 = e_1 \left(\frac{i_C}{C} - \frac{v_o}{RC} - \frac{dv_{\mathrm{ref}}}{dt} \right) \tag{7}$$

Define the virtual control law:

$$\alpha(i_L) = \frac{v_o}{R} + C\left(-k_1 e_1 + \frac{dv_{\mathrm{ref}}}{dt}\right) \tag{8}$$

where k_1 is a design parameter. Let the second error variable be:

$$e_2 = i_L - \alpha(i_L) \tag{9}$$

A composite Lyapunov function is now:

$$V = V_1 + \frac{1}{2} e_2^2 \tag{10}$$

Differentiating V and substituting inductor dynamics:

$$\dot{V} = -k_1 e_1^2 + e_2 \left(\frac{1}{L}(v_{in} - v_x) - \dot{\alpha}(i_L) \right) \tag{11}$$

where v_x is the intermediate capacitor voltage. To increase robustness, a sliding term is included in the control law:

$$D(t) = \frac{1}{v_{in}} \left[v_x + L\left(\dot{\alpha}(i_L) - k_2 e_2 - \lambda \cdot \mathrm{sat}\left(\frac{e_2}{\phi}\right) \right) \right] \tag{12}$$

where k_2, λ, and ϕ are positive control gains that determine the convergence speed and robustness of the controller. The saturation function sat(·) is employed to mitigate chattering effects commonly observed in conventional sliding mode controllers, thereby ensuring smooth control action.

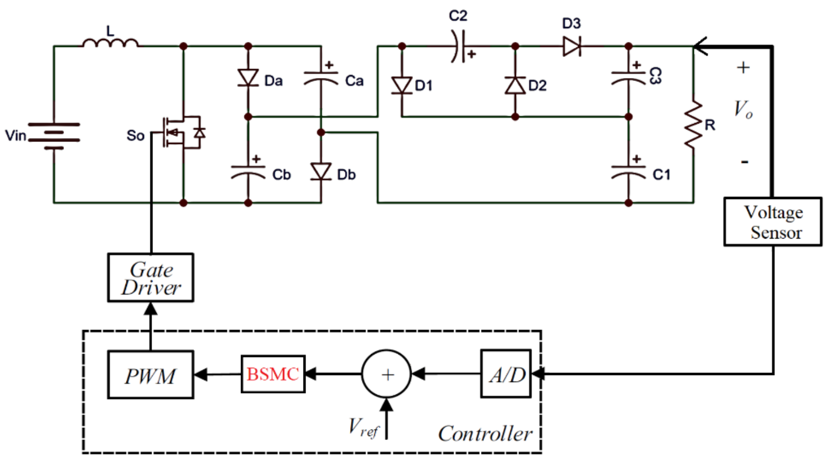

Figure 1. Block diagram overview of the CDLBC-based DC-DC converter system integrated with BSMC

Remark 3: the proposed BSMC strategy effectively addresses the control challenges posed by the nonlinear and multistage nature of the CDLBC. It provides finite-time convergence, high robustness against parameter variations, and smooth control action through the use of saturation functions to mitigate chattering. Furthermore, its software-based implementation on embedded platforms such as DSPs eliminates the need for hardware modification, enhancing its practical value and adaptability across diverse real-world applications.

To complement the theoretical formulation, the practical procedure for selecting and tuning the controller gains is outlined here. The controller gains k_1, k_2, λ, and ϕ were determined using a two-step approach. First, preliminary values were obtained from simulation sweeps to ensure stability margins and convergence of the Lyapunov function under different operating points. Second, the parameters were fine-tuned experimentally on the DSP platform to balance transient speed, robustness, and chattering suppression. Specifically, larger values of k_1 and k_2 accelerate convergence but may induce oscillatory behavior, while moderate selections of λ and ϕ effectively attenuate chattering without sacrificing steady-state precision. This combined approach provides a practical guideline for replicating and extending the proposed controller design. The derived control law outputs the switching duty ratio $D(t)$, which is applied to the PWM module of the converter to regulate the switch. This design ensures voltage tracking while preserving system stability and enhancing dynamic performance. The next section presents experimental results that validate the proposed controller under various operating scenarios.

4. EXPERIMENTAL VALIDATION AND DISCUSSION

An experimental study is carried out to validate the effectiveness and real-time performance of the proposed control strategy for the CDLBC system. The experimental setup is shown in Figure 2, which includes the constructed converter prototype, sensing circuits, control interface, and real-time data acquisition system. The controller is implemented on a Texas Instruments TMS320F28379D DSP development board, with the control algorithm designed and simulated in MATLAB/Simulink before being deployed to the hardware via code generation. The experimental setup includes capacitors C_a, C_b, C_2, and C_3, each rated at 220 μF, and C_1 with a capacitance of 470 μF. The inductor L carries an inductance of 420 μH and the resistive load adopts a value of 100 Ω. Throughout the experiments, the input voltage remains fixed at 12 Vdc to evaluate the converter's output voltage regulation under various reference transitions. In addition, to ensure consistency and reproducibility, the operating conditions were kept identical across all test scenarios. The control algorithm was executed with a sampling period of 50 μs, corresponding to a 20 kHz PWM switching frequency. Prior to each experiment, current and voltage sensor offsets were calibrated, and measurement noise was mitigated by averaging consecutive samples. These considerations clarify the boundary conditions under which the controller operates effectively. Two control approaches are compared in this study: the proposed BSMC, denoted as Method 1, and the conventional SMC, referred to as Method 2. Experimental results under different output voltage transitions are illustrated in Figures 3(a)–(c), 4(a)–(c), and 5. The voltage reference is modified in three distinct scenarios: a step-up from 35 V to 45 V, a step-up from 45 V to 55 V, and a sudden drop from 70 V to 50 V.

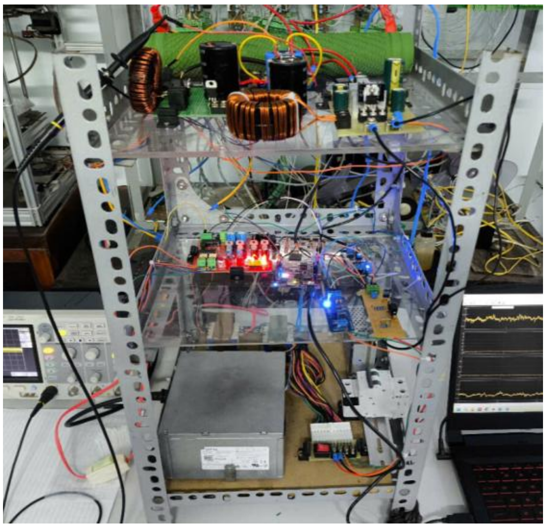

Figure 2. Experimental test setup

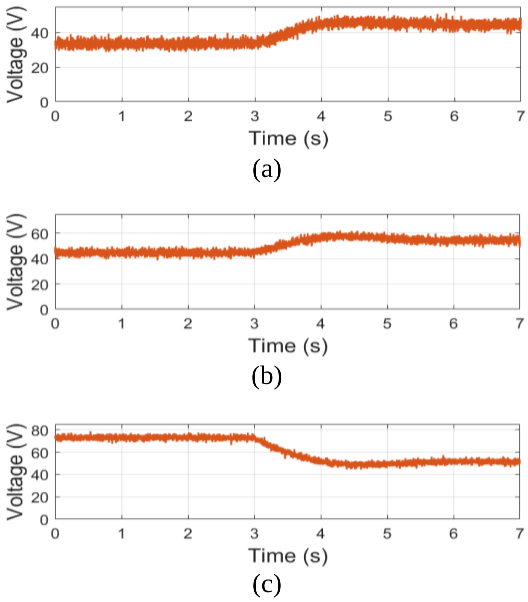

Figure 3. Output voltage response under conventional SMC method; (a) step-up from 35 V to 45 V, (b) step-up from 45 V to 55 V, and (c) step-down from 70 V to 50 V

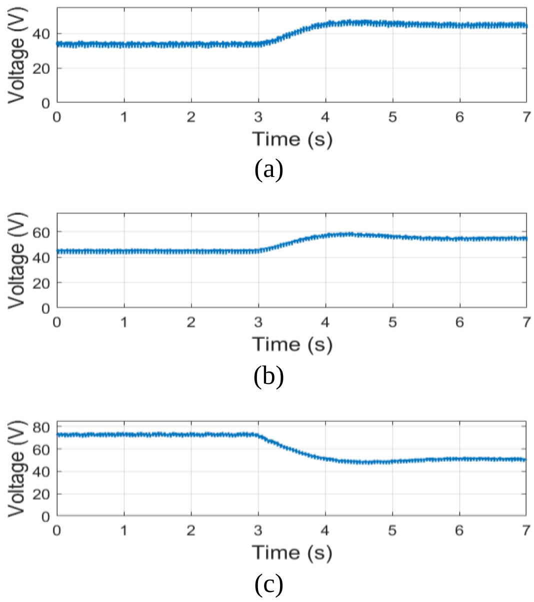

Figure 4. Output voltage response under the proposed BSMC method; (a) step-up from 35 V to 45 V, (b) step-up from 45 V to 55 V, and (c) step-down from 70 V to 50 V

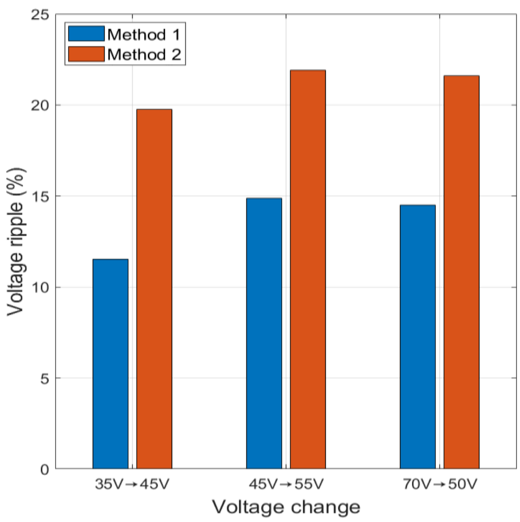

Figure 5. Comparison of output voltage ripple between conventional SMC and proposed BSMC

As observed in Figure 3, Method 2 is capable of tracking the reference voltage; however, it suffers from significant steady-state ripple and poor transient quality. The output waveforms clearly exhibit high-frequency oscillations, and the settling behavior is far from ideal. Such undesirable fluctuations not only compromise voltage stability but can also adversely impact the performance and longevity of downstream devices connected to the output. In contrast, the proposed Method 1, illustrated in Figure 4, demonstrates excellent dynamic response and significantly lower output voltage ripple across all tested scenarios. The voltage follows the reference changes more quickly, with minimal overshoot and faster settling times. This improved performance can be attributed to the adaptive nature of the BSMC strategy, which effectively handles the nonlinearities and uncertainties of the multistage CDLBC. To further quantify the quality of regulation, ripple evaluation is conducted using statistical analysis of the voltage deviation around the steady-state value. The ripple magnitude V_{ripple} is computed as $V_{\text{ripple}} = \sqrt{\frac{1}{m}\sum_{k=1}^{m}(v_o(k) - v_o^*)^2}$; where $v_o(k)$

represents the sampled output voltage at time instant k, v_o^* is the corresponding voltage reference, and m denotes the total number of samples collected over the steady-state period. Additionally, the normalized ripple percentage is defined as $\%V_{\text{ripple}} = \frac{V_{\text{ripple}}}{v_o^*} \times 100\%$. These metrics enable an objective and quantitative comparison between the two control methods.

As shown in Figure 5, the bar graph clearly demonstrates that Method 1 consistently achieves lower peak-to-peak ripple percentages across all three voltage transitions compared to Method 2. This finding validates the theoretical advantages of the proposed approach in terms of enhanced control precision and effective disturbance rejection. In addition, Table 1 summarizes the quantitative comparison of settling time, overshoot, and ripple between the two control strategies, further confirming the superior performance of the proposed BSMC. Recent studies also support these findings. For example, Huang *et al.* [11] demonstrated that disturbance observer-based composite control can significantly enhance robustness and tracking in single-stage boost converters. Although the absolute settling time of the proposed BSMC in the cascaded CDLBC topology is slightly longer, the ripple reduction from nearly 20% (SMC baseline) to about 12% remains substantial. As highlighted in [12], robustness against disturbances is still a key challenge, and most existing contributions focus on single-stage systems. By extending these advances to multistage high-gain converters, the proposed BSMC achieves improved ripple suppression and transient performance under more demanding conditions, underscoring its novelty and practical significance.

Furthermore, Figures 6(a) and (b) illustrate the transient voltage and current responses with the proposed BSMC. When the input voltage is kept constant and the reference voltage is step-wise increased, the output voltage promptly tracks the commands with high accuracy and no overshoot. The corresponding current waveforms remain smooth, exhibiting clean transitions and minimal distortion across all operating points. These results highlight the excellent damping and precision of the proposed scheme, further confirming its robustness and suitability for fast, accurate, and disturbance-resilient regulation.

Table 1. Performance comparison between SMC and BSMC

Test scenario	Controller	Settling time (s)	Overshoot (%)	Steady-state ripple (%)	Efficiency (%)
35 V→45 V	SMC	2.8	4.5	19.8	91.2
	BSMC	2	0.5	12	93.5
45 V→55 V	SMC	2	5.1	22	90.9
	BSMC	1.5	1	14.9	93.1
70 V→50 V	SMC	1.4	4.4	21.6	91.0
	BSMC	1.2	1	14	93.3

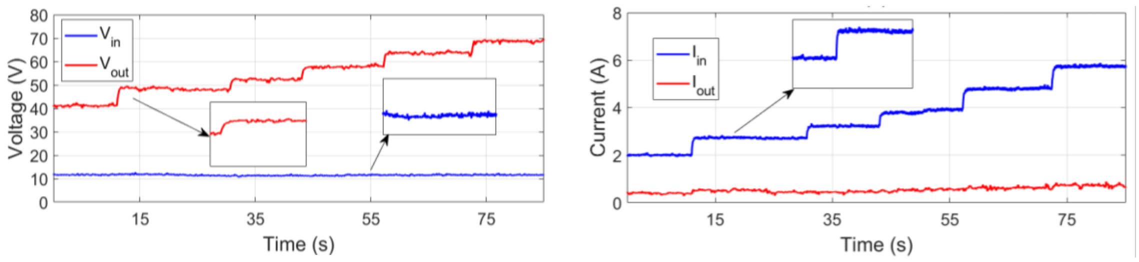

Figure 6. Voltage and current responses with the BSMC under varying reference voltage conditions; (a) input and output voltages and (b) input and output currents

The proposed BSMC strategy proves applicable beyond laboratory conditions, making it well-suited for renewable energy, electric mobility, and embedded systems where robustness and fast response are crucial. Experimental results confirm precise tracking, reduced ripple, faster settling, and no overshoot, showing clear advantages over conventional SMC. Its software-only implementation enables scalable and cost-effective integration without hardware modifications. The novelty of this approach lies in combining Lyapunov-based backstepping with sliding-mode robustness, tailored to the nonlinear multistage dynamics of CDLBCs. While computational demand is higher than linear methods, it remains manageable on the DSP platform. Future work may address sensitivity to parameter variations, measurement noise, and scalability to converters with additional stages, while also investigating switching losses, thermal effects, and EMI behavior. Moreover, optimization-based or adaptive tuning and fault-tolerant schemes could further enhance real-time feasibility and reliability in practical deployments.

5. CONCLUSION

An integrated approach that combines the inherent advantages of the CDLBC with a novel BSMC strategy is proposed for high-gain DC-DC conversion. The experimental results demonstrate that the proposed BSMC controller consistently outperforms the conventional SMC in both steady-state and dynamic performance across a range of operating scenarios. Key improvements include reduced output voltage ripple, faster transient response, and high tracking accuracy under abrupt reference changes. Notably, these enhancements are achieved through software-only implementation, eliminating the need for hardware modifications and enabling scalable, cost-effective deployment. The demonstrated robustness and efficiency make the proposed system highly suitable for next-generation applications such as residential PV systems, battery-powered electric vehicles, and portable power electronics, where adaptive control, modularity, and reliability are critical design considerations. Future work may explore the integration of intelligent tuning algorithms or fault-tolerant enhancements to further expand the system's operational envelope.

FUNDING INFORMATION

Authors state no funding involved.

AUTHOR CONTRIBUTIONS STATEMENT

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Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Thanh-Lam Le	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Nguyen Nhan Bon			✓	✓		✓	✓	✓		✓	✓			✓

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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