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Developments in scan shift power reduction: a survey

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ABSTRACT

While power reduction during testing is necessary for today's low-power devices, it also lowers test costs. Scan-based methods are the most widely used approach for testing integrated circuits (IC). Test vectors are shifted into and out of scan chains bit by bit during shift operation. The time required for shift operation dominates the test time. With the geometries shrinking (7 nm→5 nm→3 nm→1.8 nm), ICs are required to be tested for newer defects, increasing test time. The most effective way to reduce test time for scan operation is to increase the frequency of the shift operation. Reduction in shift power enables scan operation to be performed with increased frequency, reducing test time, and test cost. This paper presents a survey of techniques proposed recently for shift power reduction. Various techniques, including special flip-flop usage, segmentation, reordering, and low-pass filter, are being reviewed. The techniques are organized based on main attributes to underscore their similarities and differences. Pros and cons in terms of complexities involved in their implementation are discussed. We believe this paper will provide a point of reference for further studies in scan shift power reduction and will be helpful to both industry and academia.

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1. INTRODUCTION

With the advances in integrated circuit (IC) manufacturing technology, a complementary metal-oxide semiconductor (CMOS) IC contains billions of transistors. However, limited battery capacity, high cooling costs, and circuit reliability are only some factors that made it necessary to consider power consumption during IC design [1]. In a full scan sequential circuit, scan flip-flops replace all functional flip-flops and operate in two modes: shift and capture. In shift mode, scan flip-flops are connected as shift registers or scan chains directly accessible from a tester. This mode is used to load a test vector through shift-in or observe a test response through shift-out for the combinational portion of the sequential circuit. In capture mode, scan flip-flops operate as functional flip-flops and load the test response of the combinational portion to a test vector into themselves in preparation to shift out later in shift mode.

A circuit consumes more power in scan mode than in the normal mode since; i) a large portion of scan circuitry embedded in a circuit is often idle at any given instant during normal operation, ii) a high toggle rate is used to increase test efficiency, and iii) parallel testing is frequently employed to reduce the test application time. Average power and peak power need to be constrained due to this. Industry uses the following solutions to alleviate these constraints [2]; however, the test cost increases when these approaches are followed since they result in increased test time or using expensive equipment.

- Increase in size of power supply, packaging, and cooling: the drawback of using these solutions is that both hardware costs and test application time increases with it.

- Using reduced frequency: this increases test time, and a few of the dynamic faults might get masked, resulting in a loss in defect coverage.
- Partitioning of the chip and testing a few portions at a time instead of the whole chip: this allows for detecting dynamic faults but increases hardware overhead, test time, and total energy.

This paper presents a survey of recently proposed scan shift-power reduction techniques. Section 2 provides background and motivation for the study, while section 3 presents a classification of the techniques based on critical parameters. Sections 4 and 5 review the techniques, section 6 presents a summary and discusses the pros and cons of the techniques. Finally, section 7 concludes this paper with a discussion of future directions.

2. BACKGROUND

Generally, test power dissipation, which consists of shift and capture power dissipation, is significantly higher than functional power dissipation [3]. Excessive test power dissipation may result in permanent damage to a circuit, reduce the circuit's reliability due to accelerated electromigration, or yield loss due to faulted test results caused by IR-drop [4]. On the other hand, reducing the power dissipation increases the lifetime and reliability of the circuit [1]. Reduction in test power is also vital to improve battery life for portable electronic devices as they use periodic self-test during remote testing. For two reasons, power reduction by minimizing switching activity (SA) is the primary technique researched to reduce scan shift power: i) the signal SA could be doubled or even more in the test mode than in the functional mode [3] and ii) while reduction methods involving supply voltage and global clock period reduce circuit performance, techniques involving minimizing SA do not introduce performance degradation.

During the scan-in and scan-out phases of the scan operation, the effect of scan ripple propagates to the combinational block, which results in redundant switching. Since vectors are loaded in scan cells via serially shifting in test data bit by bit, the distribution of specified bits determines the SA in the circuit under test (CUT). It is being found that different combinations of values based on their locations have a different impact on the shift power dissipation [5]. The estimation of shift power caused by the logic value differences is calculated using weighted transition metric (WTM). The shift power in the ith test vector is estimated as (1) [6]:

$$\mathrm{WTM_i} = \sum_{j=i}^{N-1} \left(S_{i,j} \oplus S_{i,j+1}\right) \times j \quad (1)$$

where N represents the number of scan cells and $S_{i,j}$ is the logic value of the j^{th} scan cell in this test vector.

2.1. Previous surveys on low power test

Basker and Arulmurugan [7] presented a survey on low-power testing of very large-scale integration (VLSI) circuits, which summarizes power reduction techniques, including scan reordering, clock splitting, bit swapping linear feedback shift register (LFSR), and pattern generator for built-in self-test (BIST). It also describes basic x-filling techniques like 0-fill, 1-fill, and MT-fill. Another survey for test power minimization is presented in [8]. Along with shift power reduction techniques for regular-scan, it summarizes power reduction when scan compression methodologies are being used. These two surveys were presented in the years 2012 and 2013, respectively, and researchers have presented multiple techniques focussing on shift power reduction afterwords. This paper attempts to summarize those advances.

3. CLASSIFICATION

For scan testing, patterns are generated either using an automatic test pattern generator (ATPG) tool or a BIST pattern generator. Power reduction during shift mode is achieved by structural modification or optimizing the patterns. Several techniques have been presented in the literature for shift power reduction. Tables 1 and 2 provides their classification based on the common principle being used.

Table 1. Techniques for design for test (DFT) architectures using ATPG

Sr.	Technique	Type
1	Special scan cell	Structural
2	Segmentation and using non-overlapping or staggered clocks	Structural
3	Modifying scan path	Structural
4	Ordering chains based on logic connectivity	Structural
5	Ordering chains based on pattern contents	Structural
6	Ordering chains using both logic connectivity and pattern contents information	Structural
7	Pattern modification	Pattern optimization
8	Pattern reordering	Pattern optimization

Table 2. Techniques for DFT architectures using BIST

Sr.	Technique	Type
1	Counter to generate single input change (SIC) sequences	Structural
2	Low-pass filter	Structural
3	Weight-based segmentation	Structural
4	Bit-swapped LFSR	Structural
5	Biased circuitry for pattern generation	Structural
6	Target deterministic BIST	Structural

4. TECHNIQUES FOR DESIGN FOR TEST ARCHITECTURES USING ATPG

4.1. Special scan cell

Special scan cells are presented in [9]-[13]. They block the functional output going to the combinational logic during test mode, thereby reducing redundant switching during shifting. Different techniques are used to block functional output during shift operation. Figure 1(a) shows a cell that uses separate latches, while the cell in Figure 1(b) uses gated control signals to block toggling. The scan cells in [12], [13] additionally retain the last capture value. They preserve the combinational logic state when the cell changes mode from functional to shift, which helps to reorder patterns effectively for minimizing power. Though the fanout of the scan port of the cell is usually one and so redundant toggle on it during functional mode results in minimal additional power, the cell presented in [10] blocks it saving the additional power during functional operation. Special scan cell which can be used to save power during shift operation presented in [14]-[17].

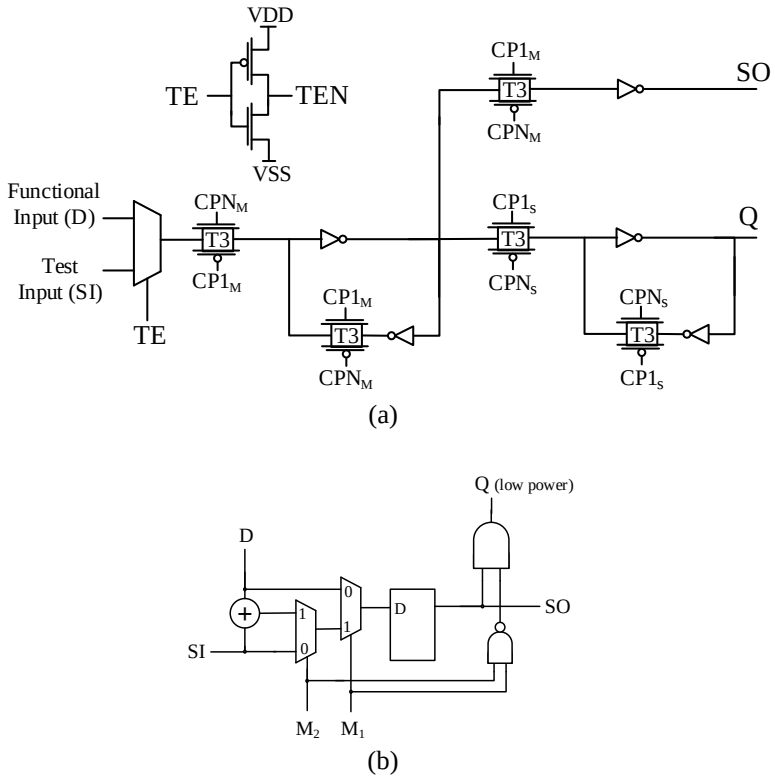

Figure 1. Scan cells with gated functional output during shifting, (a) cell with separate latches for functional and scan path [13] and (b) trimodal scan cell [11]

The cell in [9] removes the slave part in a conventional scan cell. Also, its scan path sees two fewer inverters and one less transmission gate. SA in the scan cell is minimized during shift operation due to the reduced number of cells on the scan path. The cell in [13] uses a separate path for shift purposes. The functional slave latch is disabled during the shift operation, eliminating redundant switching in combinational

logic driven by the cell during shifting and reducing toggles in the cell itself. Furthermore, the cell retains captured value after changing to shift mode, a valuable property for pattern reordering.

Cao *et al.* [10] presented a scan flip-flop with a data retention feature. It contains separate slave latches for functional and shifts purpose. The latch for shifting is also used for data retention in the sleep mode, thereby alleviating the extra area cost for test purposes. In addition, the cell eases the hold-time requirement for the test path by elongating the delay. However, one disadvantage of this cell is an increased delay in a functional path that reduces normal operation frequency. Also, the cell area is larger as it uses 16 extra transistors compared to the conventional data retention flip-flop. On the other hand, the scan cell in [18] eliminates the scan mux from a functional path, improving performance during the functional mode.

Mrugalski *et al.* [11] presented a scan cell called a trimodal scan (TMS) cell. It defines a separate compaction mode, accumulating test responses, and shifting out results every clock cycle. It uses two muxes on data path input. With control signals set to 11, output signal propagation to a CUT is prevented. This method in [11] dynamically configures scan cells in three modes: stimuli, compaction, and mission. It puts most cells in functional mode during testing, thereby saving power.

A scan cell working on a single phase of a clock for the entire operation is presented in [19]. Power consumption is reduced since the number of transitions is less than in operation with two phases. One drawback of this cell is that it has a common port for functional and test data. So redundant switching happening in combinational logic during shifting test patterns is not prevented.

4.2. Segmentation and using non-overlapping or staggered clocks

Segmentation-based techniques are most popular for reducing shift power. They are easier to incorporate into the standard implementation flow, do not add extra testing time, and only need a small extra area. It partitions the scan chain into segments that are shifted one at a time to reduce shift power. DFT architectures based on segmentation are discussed in this section. In addition to the papers listed below, papers [20], [21] also uses segmentation-based techniques.

Lee *et al.* [22] presented a segmentation technique to reduce shift power that skips segments. First, it analyses each pattern to understand which segments do not contribute to detecting a fault. Then, it processes segments serially from first to last and generates a mode control signal to skip segments that do not contribute. Further, it uses a heuristic to merge patterns with the same skip segments. Lim *et al.* [23] extended the scan segment skip technique to maximize the bypass portion. First, it analyzes patterns to note the weighted transition value for each scan cell. Then, it reorders cells according to the descending value of weight values. Finally, it reorders patterns to avoid possible chain length differences in shifting out of the pattern due to bypassing segments.

Scan architectures presented in [24], [25] split chains into multiple segments considering data dependency. During the capture operation, a selective number of segment groups are enabled in a cycle to capture the partial test response for each test pattern. Finally, the capture operation is repeated to receive a response from all segments. It starts with splitting each chain into multiple segments based on layout information. Then, it builds dependency graphs and assigns cells to segments to reduce data path crossings.

Iwata *et al.* [26] proposed using staggered clocks to reduce shift power in ultra-low power device testing. Scan testing is prone to current variations when used during power-on self-test. Moreover, significant current variations could happen at the start and end of the scan testing. To suppress these current variations, the author proposes to use a clock with a gradual increase in speed, as shown in Figure 2. After the clock frequency reaches shift speed, actual scan shifting starts.

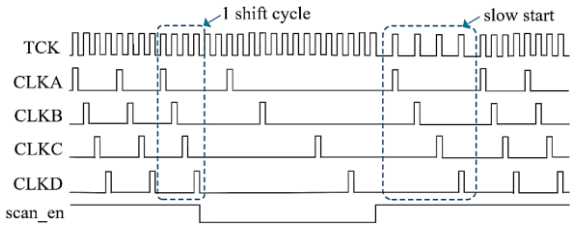

Figure 2. Staggered clock operation [26]

Segmentation techniques in [24], [25] involve cutting a functional clock into multiple branches to feed the individual segments. Unfortunately, cutting a clock creates clock divergence at the root of the functional clock tree. In addition, the added mux and clock gate increases the insertion delay on the functional clock. These overheads take a lot of design effort and add area due to clock buffering to balance

these clocks. Pradeep *et al*. [27] proposed a technique that avoids these two overheads. It uses divided and phase-shifted versions of a clock for shifting, as shown in Figure 3. It shifts data in multiple segments in parallel using such clocks. No change is made to the pattern generation methodology and patterns are generated by configuring the design for a single clock. Before testing, those patterns are modified to scramble bits. Finally, the stimulus and response data are sequenced alternatively to form a single input and output stream.

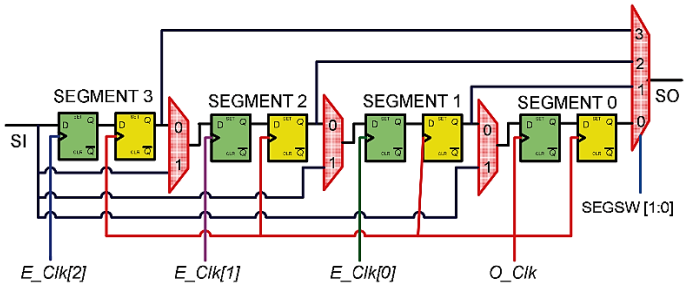

Figure 3. Scan segments with divided and phase-shifted clocks [27]

Wang *et al.* [28] presented a method to assign blocks to be used with a clock staggering technique. It considers the physical location and power supply network while assigning the blocks. For example, it does not assign two neighboring blocks that share the same power rail to a segment group, thereby avoiding toggling them simultaneously during shift. Instead, based on the location of blocks, power supply connections, and the number of wires, blocks are chosen to be driven by a staggered clock. Finally, it presents a heuristics algorithm to make optimal assignments of blocks.

4.3. Modifying scan path

A scan path modification-based methodology is presented in [29], in which an exclusive OR (XOR) gate is added at the scan input (SI) port of each flip-flop. First, it generates a pattern set by setting the XOR control line as 0. It then creates another set of patterns by transforming the initial set by setting the XOR control line as 1. Finally, toggle counting is done for each pattern in the original set, modified set, and a pattern with fewer toggles is chosen to become part of the final set. Though the method is simpler to get patterns with reduced power, it incurs a very high area overhead as one XOR gate is added per flop.

Seo *et al.* [30] presented a decompressor-multiple input signature register (MISR)-based scan architecture in which all flip-flops in a scan chain are connected to a SI port, reducing a large number of SA caused by the shifting patterns serially. Furthermore, it connects flip-flop outputs directly to scan output (SO) ports eliminating the shift-out power. Cells are divided into groups. Shift operation is enabled for one group at a time, while capture operation is performed simultaneously for all groups. A similar technique for shift power reduction is used in [25], which connects scan cells directly to SI and SO ports. Rau and Wang [31] also presented technique of modifying scan path to save power during shift operation.

4.4. Scan chain ordering

In the conventional DFT design flow, the synthesis tool assigns an instance name to each flip-flop in the netlist and the flip-flops are stitched in alphabetical order by instance name into the scan chains. However, to reduce SA in the combinational logic or in the chain itself, the ordering of cells could be changed. This section surveys the techniques that build chains to reduce shift power.

4.4.1. Ordering chains based on logic connectivity

Pathak *et al.* [32] proposed a methodology for scan stitching called logic cluster controllability (LoCCo). First, it performs circuit analysis to create combinational logic clusters between flip-flops. Then, it calculates combinations of bits required at the flops' output to test the clusters' logic. Finally, the stitching algorithm places flops with higher and lower test combinations requirements at the beginning and end of the chain, respectively. When patterns are generated with such chains, don't-care bits get clustered at the end of a chain, resulting in reduced power consumption during the loading of a pattern.

Lee *et al.* [33] presented a scan cell ordering method that considers reduction during both scan loading and unloading. Using controllability analysis, the method groups flops with similar scan-out data in the same chain. Flops are arranged in ascending order of probability of capturing 1 and 0. Chains are formed

with cells having similar probability to ensure the formation of the same bit streams in the scan chains as far as possible. The author uses the same principle as [32] to reduce shift-in power. It analyzes the fanout of cells and puts flops with greater influence at the front of scan chains and lower influence value at the end of the scan chain, as shown in Figure 4.

Zhang *et al.* [34] presented a method to create scan chain groups to be shifted one at a time instead of shifting simultaneously to reduce shift power consumption. It focuses on the problem of scan cell data retention due to excessive IR-drop during shifting test patterns. IR-drop occurs when too many flops switch simultaneously and over-stress the power delivery network. As soon as the area around the flop experiences switching above a threshold, the supply voltage to the flop may drop too low, and the flop's value may get flipped. Figure 5 depicts such data corruption. The paper presents an algorithm that considers all circuit elements, including clock tree buffers, scan cells, and combination logic gates to determine the grouping of scan cells to be tested simultaneously. The method does not use data from any test patterns. Instead, it analyzes circuit structure and cell placements to construct hypergraphs and uses a standard satisfiability (SAT) solver.

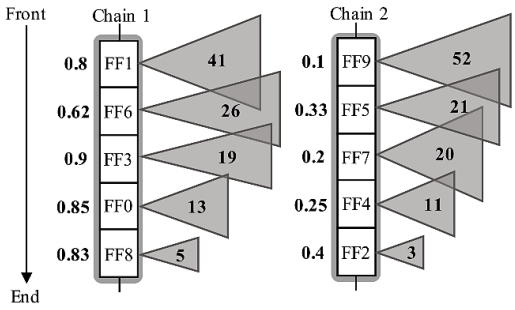

Figure 4. Scan stitching proposed in [33]

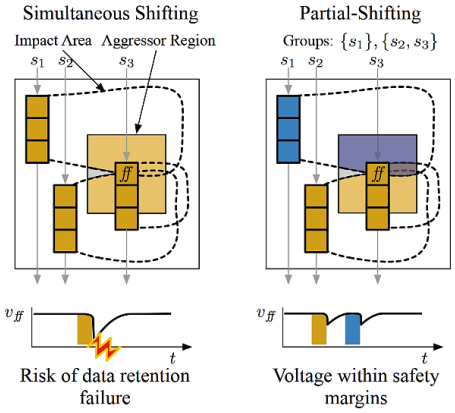

Figure 5. Data corruption due to simultaneous shifting of chains [34]

Zhang *et al.* [35] extended the technique to mitigate shift timing failures caused by excessive IR-drop on clock buffers. Similar to [34], it uses netlist and layout information. It estimates skews using proximity and defining impact area. In addition, the algorithm works towards creating groups of chains to reduce the imbalance of SA around clock paths of neighboring scan flip-flops in a chain. These test pattern-independent methods make them more practical for implementation in an actual test design flow.

4.4.2. Ordering chains based on pattern contents

Techniques presented in [36]-[38] use patterns based on default scan cell ordering. They analyze the care bits distribution in them. Later they use the information to decide the order of the cells in a chain. Cho *et al.* [36] presented a technique that generates patterns without x-filling to identify care bits for scan cells. It reorders scan chains to put cells with higher and lower care density at the beginning and end of the chain, respectively. Placing lower care bit density cells at the end of the chain results in less switching when data traverse through the chain.

The technique presented by Seo *et al.* [38] calculates the weighted hamming distance (WHD) for each scan cell. Then scan cells are arranged based on their WHD in ascending order and the stitching algorithm connects them in order. Scan cells with minimum and maximum WHD are placed at the front and end of the chain, respectively. Similarly, a technique in [37] stitches the scan cells with similar weights for logic 1 and 0's into the same scan chain.

4.4.3. Ordering chains using both logic connectivity and pattern contents information

The technique presented in [39] focuses on reducing routing overhead. It creates clusters of scan cells based on their distribution. It uses the K-means algorithm, which considers routing constraints for this purpose. The method chooses a cluster for assigning a border scan cell so that the number of transitions is less when the test patterns are applied. It evaluates the number of transitions caused by the connected scan cells during test application and reorders them to minimize it.

The technique in [40] creates partitions and assigns flops using layout information. Then, it uses initial test patterns and performs x-filling to create bit streams with similar values (either 1 or 0). Finally, it performs scan stitching using physical distance information of scan cells from DEF and WTM values calculated using patterns after x-filling.

Kim *et al.* [41] presented a scan chain architecture that creates scan segments depending on circuit topology. Figures 6(a) and (b) show an example with seven scan cells and segments created with default order for it, typically alphabetically of instance names, respectively. The proposed method reduces the shifting power by bypassing scan segments to reduce SA. First, it analyzes initial test patterns to identify scan cells with don't care values. These cells are assigned to one segment. Next, scan cells connected to the same combinational logic are classified into the same scan segment, which increases the number of segments that can be bypassed. Figure 6(c) shows partitioning for the example circuit after such analysis.

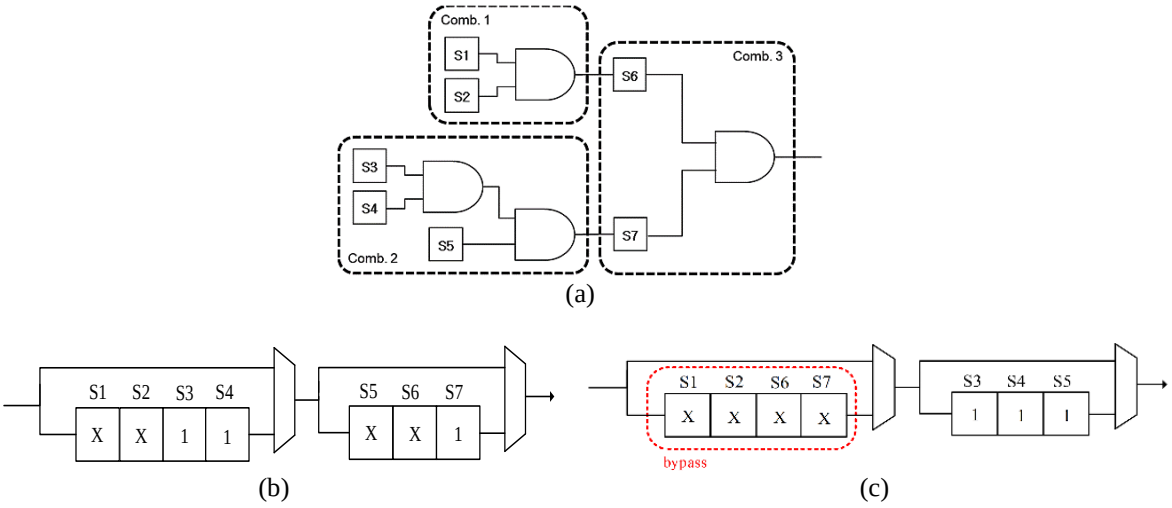

Figure 6. Scan partitioning proposed in [41], (a) example circuit, (b) partitioning with default order, and (c) partitioning with logic analysis

4.5. Pattern modification

Holst *et al.* [42] presented a pattern modification flow to reduce IR-drop-induced scan shift errors. Figure 7 lists various activities being performed in it. Excessive switching during shifting causes localized IR-drop around clock buffers and introduces delays. The method analyses the circuit to understand aggressor cells for each scan cell which affects the timing of the shift path connected between it and the predecessor scan cell. It uses initial patterns generated using ATPG and simulates them by annotating timing information. Toggle events during each cycle are noted and delays due to each are estimated using a weighted sum. Further, pattern analysis is done for delays having the potential to corrupt shift data and the vector is updated such that the scan cell with potential timing violation does not receive toggled data during the cycle. The method guarantees patterns with no shift data corruption due to IR-drop during shifting. This method is quite attractive as it is post-ATPG and non-intrusive.

Karmakar *et al.* [43] presented a dictionary-based technique to reduce shift power. Power reduction is achieved by filling the don't care bits such that transitions are minimized. However, a high compression

ratio is achieved by filling the don't care bits to get more sub-vectors, which increases the transitions. The technique performs x-filling with a trade-off between these two. First, it divides floorplan to create blocks of similar size and performs thermal simulation to create a database of power values of each logic gate in design. Then it performs x-filling on test patterns to reduce transitions with the baseline method presented in [44]. In addition, it improves the method by performing x-filling on multiple chains instead of a single chain. Further, it creates compatible slices from the patterns and uses a heuristic to get compressed patterns.

X-filling techniques offer a simple yet effective solution to reduce shift power during scan testing. The basic x-filling algorithms replace the unspecified bits with either 0 or 1 or adjacent bits, which minimizes SA. Techniques presented in [45]-[47] use these algorithms to create pattern sets with reduced shift power. It calculates power consumption for each pattern using them and chooses the patterns which produce the least switching while maintaining fault coverage.

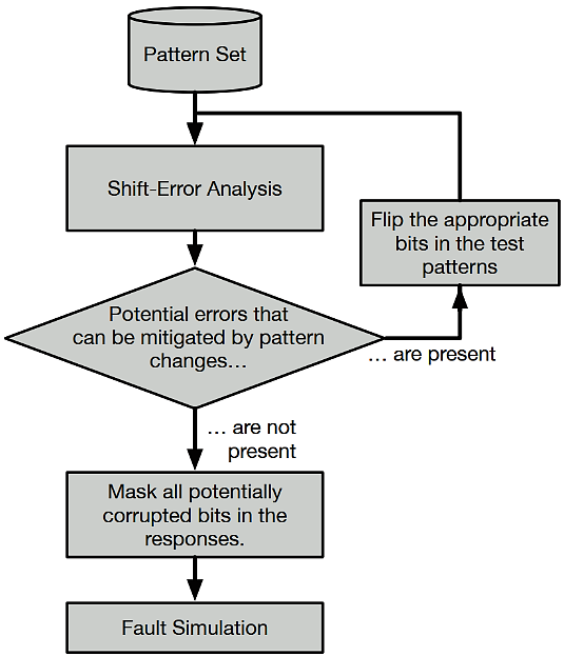

Figure 7. Pattern modification flow [42]

4.6. Pattern reordering

Maity *et al.* [48] proposed a test vector reordering technique to reduce SA in a scan chain. For a few flops, the current vector value and previous response value may be complementary, which results in significant switching when they traverse through the chain. The method uses a modified Prim's algorithm. It calculates the SA cost for each pair of vectors ordering in both directions and gives ordering with minimal test power. It splits the design into sub-blocks. It performs reordering at an inter-block level and merges the vector sets. Splitting strategy significantly improves run time and memory requirements, thereby offering advantages over clash-based and particle swarm optimization (PSO) based reordering techniques presented in [49], [50].

Kumar *et al*. [51] presented a technique to reorder patterns to reduce shift power. It calculates hamming distance between successive patterns. It starts with the first pattern as a pivot pattern and chooses a pattern with minimum hamming distance to be next in position. It performs this process for remaining patterns. Further, it uses a second pattern from the original set as a pivot and creates another set of patterns. It creates such sets by treating each pattern as a pivot. Finally, it selects the set having minimum global hamming distance.

5. TECHNIQUES FOR DFT ARCHITECTURES USING BIST

BIST-based testing offers advantages over ATPG in terms of the ability to do remote testing and testing for unmodelled faults. LFSRs are the most widely used test pattern generator due to their small size and ability to generate unique patterns. However, being pseudo-random, consecutive patterns generated by LFSR have a very low correlation, resulting in high SA [3]. Like pseudo-random LFSR-based BIST, deterministic BIST also results in high toggle activity during shifting. Several techniques have been proposed

to reduce this switching. While most papers focus on switching reduction in circuits employing puedo-random LFSR-based BIST, few papers also present techniques for deterministic-BIST-based circuits. This section provides a review of recently proposed techniques.

5.1. Counter to generate single input change sequences

Margade *et al.* [52] presented a technique to reduce shift-in power while testing using a logic built-in self-test (LBIST). The technique uses the Johnson counter to generate a SIC bit stream. It contains an LFSR-based seed generator to create unique patterns. Outputs of LFSR and Johnson counter are XOR'ed and fed to the scan chain as a test pattern. Since patterns fed to chains have low input transitions, shift-in power is reduced. Later a technique that also uses Johnson counter to reduce power is presented in [53].

One drawback of using a random-single input change (RSIC) generation method based on LFSR is an increase in test length. Also, the seed needs to be carefully chosen [54]. Cao *et al.* [55] presented a sequential single input change (SSIC) sequence generation based on deterministic BIST to lower power during shift. The SIC test sequence is created based on ATPG. The method generates an input bit stream in an orderly manner. It uses a counter instead of a pseudo-random source LFSR and inverts the vector bit sequentially in each test cycle. Due to its deterministic nature, SSIC-generated sequences achieve better fault coverage than RSIC-based sequences.

5.2. Low-pass filter

A pseudo-low-pass-filter (PLPF) suppresses the toggle rate by taking the moving average of the SI bit stream [56]. Figure 8 shows two of such filters. Kato *et al.* [57] presented a technique to reduce power which controls the toggle rate of pseudo-random patterns. The proposed method inserts a PLPF with fewer logic gates between a scan chain and a phase shifter for filter (PSF) as shown in Figure 8(a). The output of this PLPF toggles when a past bit is different from both input values. It ignores toggles occurring at the current and future bit of PSF.

Bhandari *et al.* [58] presented another variant of the random toggle rejects circuit. The random reject circuit is added for each shift register stage of LFSR. The output of two consecutive registers is given to these circuits as shown in Figure 8(b). This circuit partially fixes bit values to produce correlated adjacent bit sequences. Further, the method uses a complimentary version of signals as data output, which helps reduce LFSR's size requirement.

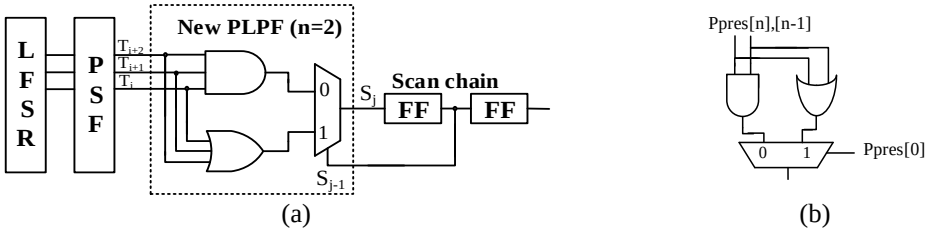

Figure 8. Low-pass filters, (a) filter with mux select from scan chain [57] and (b) filter with mux select from LFSR stage [58]

5.3. Weight-based segmentation

Issa *et al.* [59] presented a weight-based segmentation technique to reduce power during BIST pattern application. It calculates the scan cell's weight 1 (or 0) by finding a ratio of the number of test vectors where the cell is 1 (or 0) to the total test vectors. Cells with similar weights are connected in the same scan chain. Using weights increases the likelihood of generating needed tests for detecting faults. Further, it replaces XOR gates in the phase shifter with a simple combinational circuit. The biased circuit helps to get high fault coverage in the shorter test length as well as reduces the number of transitions while loading a bit stream in a scan chain. Techniques presented in [57]-[60] also fall under the category of biased circuits.

Filipek *et al.* [60] presented a DFT architecture, as shown in Figure 9. It produces binary sequences with a preselected toggling (PRESTO) rate. The toggle rate is chosen using a value in a control register called switching, which is loaded once per pattern. It also allows the scan chains to be driven by constant values instead of professional rules and practice guidelines (PRPG) for a given period, providing additional flexibility to create low transition patterns. The DFT architecture provides a hybrid test solution that

combines LBIST and ATPG-based embedded test compression. Due to the deterministic nature of the BIST, a highly efficient pattern set could be generated using the solution.

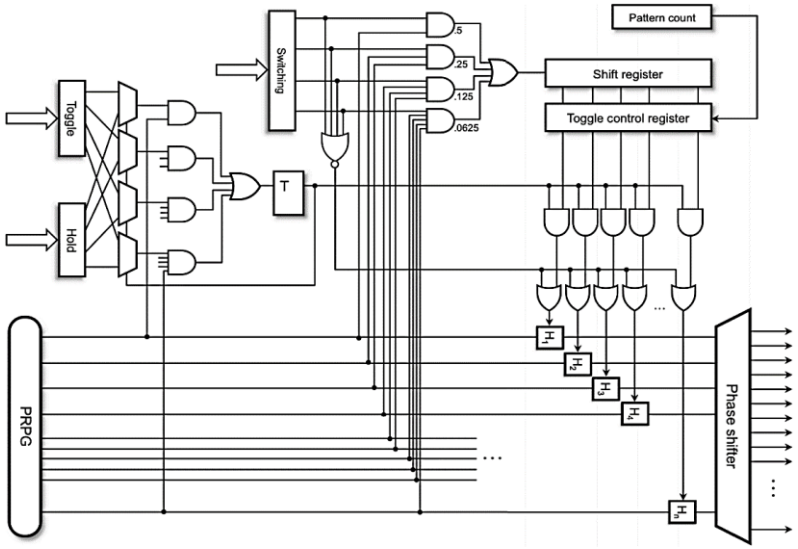

Figure 9. Hybrid test solution [60]

Shivakumar *et al.* [61] presented a weighted pseudo-random test pattern generator to reduce power during the BIST. It uses the Galois scheme and provides particular weights to the respective scan chains through the weighted mux. The test patterns are generated concurrently using the shift registers and Galois operation, producing low stitching transition patterns and improving fault coverage. Xiang *et al.* [62] proposed a weighted pseudo-random pattern generation method to reduce power. It analyzes cost by assigning weights to each scan chain and choosing the optimal value. Further, it activates only a small number of scan chains in a single cycle and feeds constant data to disabled chains. Sankari and Maheswari [63] also presented a weight based segmentation technique to save power during shift operation.

5.4. Bit-swapped linear feedback shift register

Bit-swapping LFSR reduces the number of transitions in SI being applied to CUT. The technique swaps the value of a cell with its adjacent cell's value if the current value of the third cell in LFSR is 0 and leaves it unchanged if it is 1. Transitions due to two cells can be reduced by 25% using a swapping method [64]. Sharan *et al.* [65] presented a design, as shown in Figure 10, to reduce power during BIST pattern application. It uses a bit-swapped LFSR and a modified MISR to generate low transition patterns.

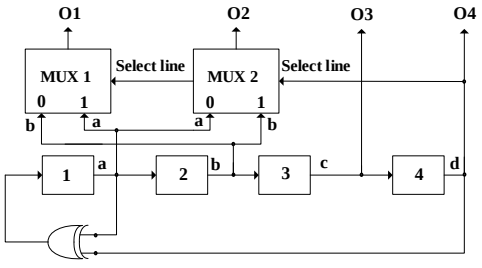

Figure 10. Bit-swapped LFSR [65]

6. DISCUSSION

Several techniques to reduce scan shift power have been described in sections 4 and 5. Table 3 and 4 lists the techniques alongwith references. Few papers presented multiple techniques and those techniques are listed as separate entry in respective type. This section presents summary of them.

Table 3. Techniques for DFT architectures using ATPG

Sr.	Technique	Type	References
1	Special scan cell	Structural	[9]-[19]
2	Segmentation and using non-overlapping or staggered clocks	Structural	[20]-[28]
3	Modifying scan path	Structural	[25], [29]-[31]
4	Ordering chains based on logic connectivity	Structural	[32]-[35]
5	Ordering chains based on pattern contents	Structural	[36]-[38]
6	Ordering chains using both logic connectivity and pattern contents information	Structural	[39]-[41]
7	Pattern modification	Pattern optimization	[42]-[47]
8	Pattern reordering	Pattern optimization	[48]-[51]

Table 4. Techniques for DFT architectures using BIST

Sr.	Technique	Type	References
1	Counter to generate SIC sequences	Structural	[52]-[55]
2	Low-pass filter	Structural	[56]-[58]
3	Weight-based segmentation	Structural	[59]-[63]
4	Bit-swapped LFSR	Structural	[64], [65]
5	Biased circuitry for pattern generation †	Structural	[57]-[60]
6	Target deterministic BIST †	Structural	[55], [60]

†Sections 4 and 5 do not contain separate sub-sections for these techniques. They are covered as part of other sub-sections

6.1. Techniques for design for test architectures using automatic test pattern generator

6.1.1. Structural type

Structural modification techniques block flop output or use special flops. They increase circuit area and degrade performance.

- Segmentation techniques do not add blocking logic to the stimulus path; thus, the performance of the design is not affected. Moreover, these techniques reuse test sets generated for standard scan architectures; hence, it does not require unique ATPG algorithms. They reduce average power effectively. They require careful planning; however, they are easier to implement and well-supported by commercial computer-aided design (CAD) tools. They provide the most efficient solutions regarding shift-power reduction, integrability into existing design flows, area, and testing time overhead compared to other approaches.
- Techniques involving building chains based on logic or modifying scan paths require using a unique algorithm and require high computational times.
- Scan chain reordering methods offer an effective solution to reduce shift power. It does not add any extra logic apart from area overhead due to wire length increase which can be reduced using an efficient layout synthesis tool. Furthermore, it does not have any impact on test coverage and test time.

6.1.2. Pattern optimization type

These are attractive techniques to reduce shift power as they are post-ATPG and do not incur any circuit performance degradation. However, it requires developing an algorithm to process toggle events and use layout information to estimate delays due to them.

- The x-filling techniques offer a simple solution and are well supported by commercial CAD tools. However, one of the limitations they suffer is when a compression circuit is added to the design. Test generation methodology supports low power shift patterns using them, but their effectiveness is limited as filling the don't care bit process also needs to satisfy the compression algorithm.
- Pattern reordering techniques do not cause any overhead but require using a special algorithm and require huge computation time to process larger designs' patterns.

6.2. Techniques for design for test architectures using built-in self-test

The techniques based on low-pass filter uses extra gates to get more correlated patterns. The drawbacks of these techniques are; i) lower fault coverage since some random features are lost in these patterns and ii) increased test application time.

- The hybrid test solution [60] is a viable technique as it uses deterministic compression and is well supported by a commercial CAD tool.
- Techniques using weighted scan segments produce biased test patterns. They offer the advantage of reducing test application time since fault coverage will be achieved using lesser patterns compared to pseudo-random patterns.
- Techniques using low-pass filters add gates and muxes on scan chain input. Typically, they add 2 to 4 levels of logic which increases delay and reduces the frequency of shift operation, in addition to an increase in area overhead.

6.3. Guiding principles

Each technique offers unique benefits. They have certain limitations as well. So, it is crucial to understand them. When selecting a technique, the following constraints could be used as the guiding principles: i) performance degradation of system functionality in terms of area and operating speed, ii) increase in test time or decrease in fault coverage, and iii) compliance with the design flow for implementation.

7. CONCLUSION

The revolution of system on chip (SoC) has brought new challenges to both functional and test power dissipation. In test mode, excessive SA causes high power dissipation, overheating, and damaging the circuit. The SA rate is the primary limiting factor in determining maximum shift frequency and a reduction in it enables scan operations to be performed with increased frequency, resulting in saving test costs. This paper presented a survey of techniques for reducing scan shift power. A classification of techniques was presented, their limitations, and possible solutions were discussed. Each method has operational limitations, but a framework can be developed to use a combination of techniques.

Though partitioning techniques appear efficient, most do not avoid switching in combinational logic. Reducing these redundant switching would be future research. Scan chain reordering methods offer an effective solution. However, currently available commercial CAD tools still need to offer solutions to implement algorithms that derive the optimum order of scan cells which could be another future research area.

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