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Memory faults using open and short defect models for nano technology applications

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ABSTRACT

As technology progresses from sub-micron to nanometer scales, memory-based systems are increasingly prone to faults. Consequently, developing robust methodologies to achieve defect-free embedded static random-access memory (SRAM) has become a critical challenge in modern very large scale integration (VLSI) design. Also, the increased integration of layout layers leads to form unknown defects. From the existing literature, observed that huge parametric variation is present whenever technology is changed. This is the key issue addressed in this paper, by representing an analysis on the impact of open and short defect models that uses parasitic extraction method while drawing various fault models. Possible open/short defects between the existing nodes are considered for the development of fault models using 45 nm, 32 nm, and 7 nm technologies. The total number of fault models of both kinds observed are 147. Also observed that besides to the existing faults, few undetectable faults are found named as undefined short faults (USF), undefined write after read fault (UWARF), and few faults with multiple faulty behavior.

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1. INTRODUCTION

Faults in static random-access memory (SRAM) are mere interpretation of a failure at the manufacturing phase [1]-[3]. In order to get observe the functionality correctness various test methods are to be applied. Most of the research dealt with March algorithms found efficient in using them as test methods [4]-[6]. Traditional and March tests are used as an example for step by step procedural method while targeting particular faults in the selected SRAM structure [7]. Defects in SRAM are generally categorized as single cell and multiple cell faults. Hence algorithms are applied based on type the test cell under consideration. Single cell faults are simple in detection when the fault are static in nature. However, the static fault needs fewer operations in testing them. But, dynamic faults in the single cell rely on multiple sequence of operations to detect the fault [8], [9]. In contrast, multiple cell faults deals with more than one cell, hence the fault types are either linked or unlinked. Linked faults means once create disturbance in other cell while performing any read or write operation [10]-[12] however, unlinked faults are similar to single cell faults but appear in more than one cell at a time. Using March primitive notations all kind of single cell static and dynamic faults can be modeled. From the existing literature one can notice the March algorithms used with the complexity of 4 n to 100 n [13]-[16] in elevating the faults from any corner of the memory architecture. Most of the memory built-in self-test (MBIST) architectures uses different fault models from small to large capacity [17], using

techniques like microcode based built-in self test (BIST) [18] to address various issues like static noise margin, low supply voltage, read, and write stability. In all these memories, if one parameter is violated during system operations, it leads to erroneous behavior that causes the system to be faulty. Hence advanced test methods that are independent of technological are always essential to ensure the correctness in the functionality of the system prior to the use.

Some faults are dynamic faults that appear only during specific operation, such dynamic fault detection needs more complex primitive algorithms like FRDD [19] that may leads to more test time along with test complexity for larger memory sizes. This problem of large primitive test complexity is addressed with variable length test sequences keeping fault coverage high [20]. Due to scale-down technologies, large memory architectures have been dominated compared to their core logic area that influences the process parametric variations such as voltage lowering, changes in capacitance and resistances. Parametric variations often cause performance deviations, leading to faulty circuit behavior that is difficult to detect using conventional test techniques. Moreover, certain faults arising from process variations in sub-micron memory models remain undetectable through traditional methods. To address this, resistive-open/short defect models combined with parasitic extraction have been employed [21]. In this approach, parasitic resistance and capacitance at faulty nodes are identified and subsequently utilized for fault diagnosis, enabling both detection and localization of fault occurrences. The existing literature focused on 180 nm to 90 nm. But lower technologies use very narrow closer traces. As capacitance is inversely proportional to the distance between conductors, hence the chance of parasitic values will differ at lower technologies. Hence it essential to use parasitic extraction approach at mere lower technologies. Rest of the paper is organized in such a way that, section 2 deals with review on existing method parasitic extraction for short defect models. Section 3 continued with proposed open defect models and corresponding R, C extracted values. Section 4 analysis on the result obtained, comparison, and finally section 5 ends with conclusions.

2. REVIEW ON RELATED WORK

In general, traditional SRAM cell comprises core five nodes such as true node Q, complementary node QB, true output node BL, and complementary output node bit line bar BLB along with word logic line WL. To activate the cell, it needs supply rails connected through nodes voltage drain-drain VDD, and voltage source-source VSS. The shorts among all the nodes results in short-fault model as shown in Figure 1. For each fault model the corresponding layout should be extracted. Using circuit simulator, the fault models were drawn, and corresponding layout is extracted. As an example, when a short defect is imposed between WL and BLB, makes the cell internal value become inactive for any new value to write. Hence Q and QB are shown in undefined state during that period as shown in Figure 2. After write operation is performed, the read operation is initiated by pre-charging both the bit lines. While asserting WL line the cell stores logic 1 for short duration and the cell value will flipped from logic 1 to logic 0. This type of fault is very hard to implement using primitive representation but is possible to differentiate by extracting the node parasitic R, C values.

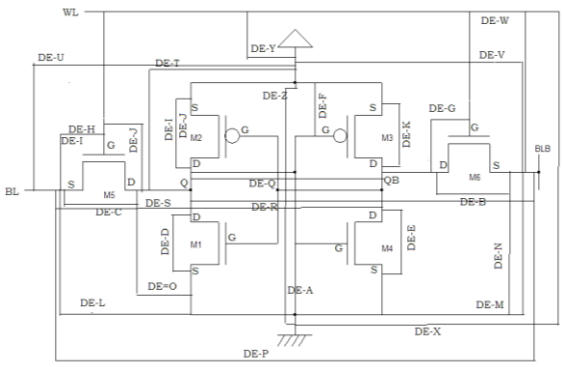

Figure 1. Representation of shorts among all the nodes results in short-fault models

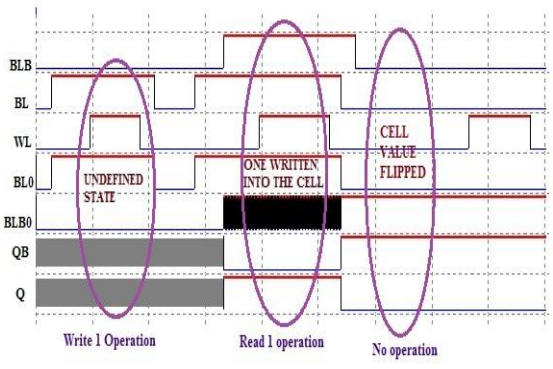

Figure 2. Simulation results observed for undefined short fault (USF) at nodes WL-BLB

Issues identified with the existing parasitic extraction test method are such that it is restricted to the application of short defects with the technologies of 180 nm, 120 nm, and 90 nm. But the behavior of faults will vary with the lower technologies. Hence the proposed method of parasitic extraction is extended to open defects, also the technologies chosen are for deep submicron level such as 45 nm, 32 nm, and 7 nm.

3. PROPOSED METHOD OF TESTING BY PARASITIC EXTRACTION USING OPEN DEFECTS AT DEEP SUB MICRON TECHNOLOGIES (45 nm, 32 nm, and 7 nm)

3.1. Testing by parasitic extraction method for short defect models at sub-micron technologies

Initial work is carried out using short defect models, but at chosen technologies such as 45 nm, 32 nm, and 7 nm shown in Table 1. The faults under observation at these lower technologies of are different from the faults that are observed in the previous work [21]. The new fault observed in this work is undefined write after read fault (UWARF) is resulted from the short defect created between WL and BLB nodes, which is a combination two or three faulty behavior of write before access fault WBAF and undefined state read fault USRF. Also noticed that few of the short defect models such as $SD_{4,5}$ and $SD_{18\text{-}21}$ have resulted different behavior while subjected to sensitization the read and write operations and are treated as no access fault (NAF).

Table 1. Proposed short defect fault models for 6T SRAM cell at chosen technologies

S. No	Defect name	Short defect at nodes	Technologies under consideration		
			45 nm	32 nm	7 nm
1	SD_2	WL-BL	SA1	TF	WBAF, TF
2	SD_3	WL-BLB	USF	USRF-1	WBAF, USRF-1 (UWARF)
3	SD_4	WL-VDD	Error (NAF)	Error	Error
4	SD_5	WL-VSS	Error (NAF)	Error	Error
5	SD_{14}	QB-BLB	WBAF	WBAF, USWF0, USRF0	USWF0, USRF0
6	SD_{18}	BL-VDD	Error (NAF)	Error (NAF)	Error (NAF)
7	SD_{19}	BL-VSS	Error (NAF)	Error (NAF)	Error (NAF)
8	SD_{20}	BLB-VDD	Error (NAF)	Error (NAF)	Error (NAF)
9	SD_{21}	BLB-VSS	Error (NAF)	Error (NAF)	Error (NAF)

3.2. Testing by parasitic extraction method for open defect models at sub-micron technologies

Furthermore, this work is extended to open defect fault models in SRAM. Initially, the concept of open defect fault modeling was explored in the context of interconnect defect models for large fanout stems [22]. The proposed open defect fault model for SRAM, shown in Figure 3, incorporates all possible open defects. Each node is disjuncted with other node to propose fault model. It is observed that totally 25 open defect models which results in various faults among which few are existing and few are fully undefined. Open defect Faults are symbolized as abbreviation for open fault (OF) in the forgoing text in this paper. Using 32 nm and 7 nm technologies, various faults that are observed by developing corresponding fault models are listed in Table 2.

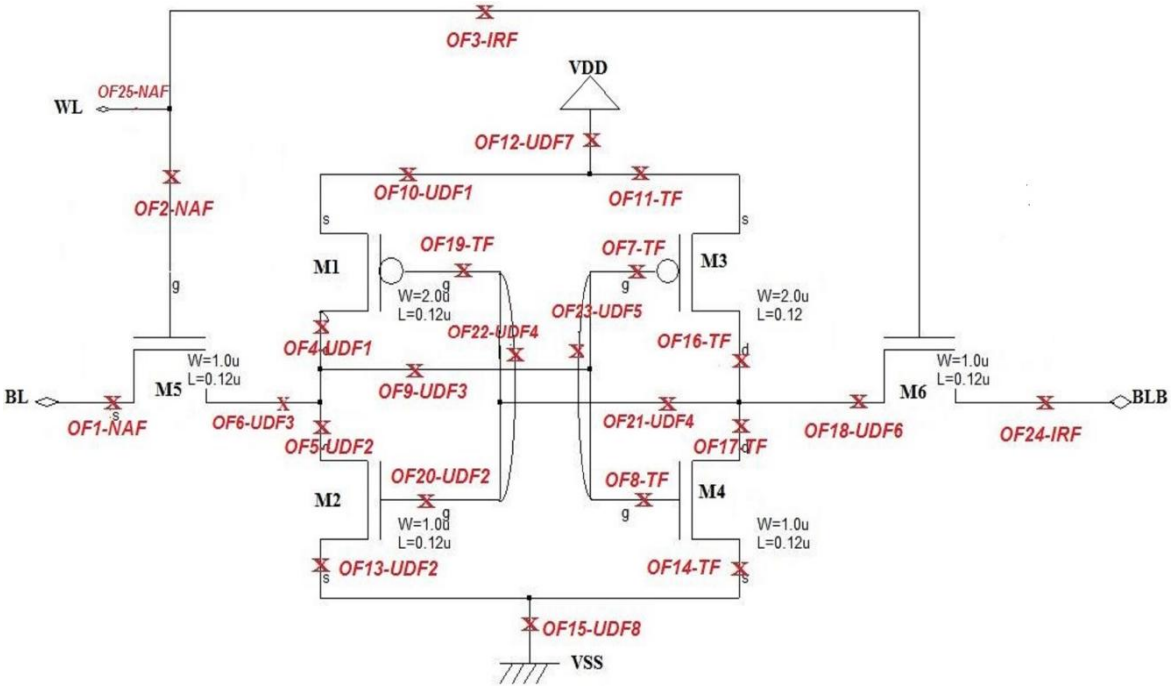

Figure 3. Fault model for open defect faults in 6T SRAM cell

Table 2. Open defect fault model list for the chosen technologies in 6T SRAM cell

Defect representation	Open defect at nodes	Technology nodes under consideration for open defects 32 nm	7 nm
$OF_{1,2,6,9}$	(BL-T_5S), (WL-T_5G), (Q-T_1DT_2D), (Q-T_3GT_4G)	NAF	NAF
$OF_{3,4}$	(WL-T_6G), (Q-T_1D)	URF	URF
$OF_{5,13}$	(Q-T_2D), (VSS-T_2S)	UWF0	UWF0
$OF_{7,8,11}$	(Q-T_3G), (Q-T_4G), (VDD-T_3S)	TF	UWF0, URF0
OF_{10}	VDD-T_1S	UWF1	UWF1
OF_{12}	VDD-T_1ST_3S	UWF, URF0	UWF, URF0
OF_{14}	VSS-T_4S	TF	UWF1, URF1
OF_{15}	VSS-T_2ST_4S	UWF, URF1	UWF, URF1

4. RESULTS AND COMPARISONS

For the proposed open and short defect fault models the experimental setup used with three lower technologies such as 45 nm, 32 nm, and 7 nm. Hence technology variation from 180 nm down to 7 nm are taken into consideration. Each technology node environmental process parameters are different, and collectively shown in Table 3. The main process parameter is lowering voltage. It is 2 v for 180 nm and 0.8 v for 7 nm technology. The other important parameter that shows great change with respect to technology is maximum operating current I_{max} (mA), that is in the range of 0.6 to 0.04. Other parameters represent widths of n and p MoS transistors.

Table 3. Process parameters for different technologies [23]

Parameter	180 nm	120 nm	90 nm	65 nm	45 nm	32 nm	14 nm	7 nm
VDD (V)	2	1.2	1	1	1	1	0.9	0.65
Imax (mA)	0.6	0.5	0.1	0.1	0.08	0.07	0.03	0.04
ML (um)	0.18	0.12	0.1	0.07	0.05	0.03	0.016	0.007
MNW (um)	1.5	1	0.5	0.3	0.3	0.08	0.048	0.024
MPW (um)	1.5	2	1	0.5	0.5	0.108	0.048	0.024

Each technology is represented with the minimal channel length that can be fabricated. For example, if it is 180 nm, the channel length to be considered as 0.18, if it is 7 nm then the channel length should be taken as 0.007. In our work the chosen technologies for experimental setup are 45 nm, 32 nm, and 7 nm. Each open defect model is simulated in circuit editor, and extracted corresponding faulty layout. From the extracted layout, the defect model is captured using parasitic R, C subjective to each node. Further these defect model parameters are compared with fault free SRAM layout to generate fault model dictionary. In the proposed work, under 45 nm technology, in addition to the existing faults, few undefined faults presence also noticed. As mentioned in the earlier sections, short between WL-BLB for 45 nm technology resulted as UWARF. But when the technology is migrated to 32 nm, the same defect model resulted as unstabilized read fault (URF). And also, when working with 7 nm, the same defect model resulted as write before access faults (WAF) during write operation and URF during read operation. In the similar line, defect model using short between WL and BL resulted as stuck at faults (SAF) in 45 nm, but in the other two technologies it resulted as transition faults (TF), and write before access faults (WBAF). Few of the other defect models like QB-VSS, and WL-BLB followed the same. With respect to open defect models, NAF is resulted when an open occurs between the nodes BL and source line of the transistor T_5, where node BL is held in hang state.

4.1. Fault model dictionary for proposed open defect fault models using 32 nm technology

The outcome of our work is to provide a complete fault model dictionary using proposed open defect fault models with their parasitic R and C values developed at 32 nm technology for 6T SRAM cells, shown in Tables 4 and 5 respectively.

4.2. Fault model dictionary for proposed open defect fault models using 7 nm technology

In the similar line defect models using 7 nm technology are developed. In the open defect model, when high impedance path is created between WL and gate of access transistor M6, results in formation of URF, with the parasitic R, C values at the faulty node are 0.52 fF, and 155 ohms respectively. However, the fault free SRAM results with parasitic R, C of 0.77 fF, and 296 ohms respectively. The corresponding fault model dictionary using 7 nm is shown in Tables 6 and 7.

From Tables 4-7 it is observed that parasitic capacitances and resistances are lowered as the technology goes down from 32 nm to 7 nm. Also, the faulty behavior is not consistent with technology variations. Compared with the outcomes of existing March algorithms [24] and the new March AZ algorithm

[25], the proposed fault detection method based on parasitic extraction achieves an improved number of detected faults with 100% fault coverage, while also offering the advantage of a technology-independent architectural consideration for the SRAM under test.

Table 4. Complete fault model dictionary for proposed open defect fault models with parasitic R values using 32 nm technology for 6T SRAM cell

S. No	Open defect between nodes	Fault models observed	At Q R Ω	At QB R Ω	At WL R Ω	At BL R Ω	At BLB R Ω	At VDD R Ω	At VSS R Ω
	Fault free		433	1170	180	158	54	2071	402
1	BL-T_5S	NAF	1583	-	178	157	53	2071	402
2	WL-T_5G	NAF	433	1170	-	236	54	2071	402
3	WL-T_6G	URF	433	1170	219	159	-	2071	402
4	Q-T_1D	UWF1	-	-	-	-	-	2164	402
5	Q-T_2D	UWF0	-	-	-	-	-	2071	553
6	Q-T_1DT_2D	NAF	565	803	-	157	54	2071	402
7	Q-T_3G	TF	433	-	1331	157	54	2071	402
8	Q-T_4G	TF	433	1170	180	158	54	1670	805
9	Q-T_3GT_4G	NAF	-	971	178	158	54	2409	402
10	VDD-T_1S	UWF1	-	971	178	158	53	2071	743
11	VDD-T_3S	TF	407	-	178	157	54	2787	402
12	VDD-T_1ST_3S	UWF, URF0	407	-	178	157	53	2071	1146
13	VSS-T_2S	UWF0	445	803	180	157	-	2071	402
14	VSS-T_4S	TF	407	842	180	157	-	2071	402
15	VSS-T_2ST_4S	UWF, URF1	-	1170	180	529	54	2071	402
16	QB-T_3D	TF	407	-	180	941	54	2071	402
17	QB-T_4D	UWF1, URF1	407	803	180	196	-	2071	402
18	QB-T_3DT_4D	URF0, UWF	-	-	-	-	-	2198	402
19	QB-T_1G	UWF1	-	-	-	-	-	2071	528
20	QB-T_2G	UWF0	-	-	-	-	-	2101	402
21	QB-T_1GT_2G	UWF	-	-	-	-	-	2071	430

Table 5. Complete fault model dictionary for proposed open defect fault models with parasitic C values using 32 nm technology for 6T SRAM cell

S. No	OD	Fault model	At Q C, fF	At QB C, fF	At WL C, fF	At BL C, fF	At BLB C, fF	At VDD C, fF	At VSS C, fF
	Fault free		2.9	3.1	1.8	1.1	0.78	2.7	1.7
1	BL-T_5S	NAF	5.5	-	1.8	1.0	0.75	2.7	1.7
2	WL-T_5G	NAF	2.9	3.1	-	1.6	0.78	2.7	1.7
3	WL-T_6G	URF	2.9	3.1	2.1	1.0	-	2.7	1.7
4	Q-T_1D	UWF1	-	-	-	-	-	2.8	1.7
5	Q-T_2D	UWF0	-	-	-	-	-	2.7	2.7
6	Q-T_1DT_2D	NAF	4.0	3.1	-	1.0	0.75	2.7	1.7
7	Q-T_3G	TF	2.9	-	4.3	1.0	0.75	2.7	1.7
8	Q-T_4G	TF	2.9	3.1	1.8	1.0	0.78	2.4	2.0
9	Q-T_3GT_4G	NAF	-	3.0	1.8	1.0	0.78	3.6	1.7
10	VDD-T_1S	UWF1	-	3.0	1.8	1.0	0.75	2.7	3.1
11	VDD-T_3S	TF	2.9	-	1.8	1.0	0.75	4.0	1.7
12	VDD-T_1ST_3S	UWF, URF0	2.9	-	1.8	1.0	0.75	2.7	3.5
13	VSS-T_2S	UWF0	3.1	3.1	1.8	1.0	-	2.7	1.7
14	VSS-T_4S	TF	2.9	3.4	1.8	1.0	-	2.7	1.7
15	VSS-T_2ST_4S	UWF, URF1	-	3.1	1.8	2.9	0.78	2.7	1.7
16	QB-T_3D	TF	2.9	-	1.8	3.5	0.78	2.7	1.7
17	QB-T_4D	UWF1, URF1	2.9	3.1	1.8	1.3	-	2.7	1.7
18	QB-T_3DT_4D	URF0, UWF	-	-	-	-	-	2.8	1.7
19	QB-T_1G	UWF1	-	-	-	-	-	2.7	1.8
20	QB-T_2G	UWF0	-	-	-	-	-	2.8	1.7
21	QB-T_1GT_2G	UWF	-	-	-	-	-	2.7	1.7

Table 6. Complete fault model dictionary for proposed open defect fault models with parasitic R values using 7 nm technology for 6T SRAM cell

S. No	Open defect between nodes	Fault model observed	At Q R Ω	At QB R Ω	At WL R Ω	At BL R Ω	At BLB R Ω	At VDD R Ω	At VSS R Ω
	Fault free		800	498	296	71	91	13	13
1	BL-M5S	NAF	805	498	296	-	87	13	13
2	WL- M5G	NAF	813	498	159	70	91	13	13
3	WL- M6G	URF	813	498	155	71	91	13	13
4	Q-M1D	UWF1	682	498	296	71	91	13	13
5	Q-M2D	UWF0	755	498	296	71	91	13	13
6	Q-M1DM2D	NAF	80	498	293	71	91	13	13
7	Q-M3G	TF	527	498	296	71	91	13	13
8	Q- M4G	UWF1, URF1	551	498	296	71	91	13	13
9	Q-M3GM4G	NAF	257	498	296	71	91	13	13
10	VDD-M1S	UWF1	711	511	296	71	91	13	13
11	VDD-M3S	UWF0, URF0	813	511	296	71	91	13	13
12	VDD-M1SM3S	UWF, URF0	711	511	296	71	91	13	13
13	VSS-M2S	UWF0	800	511	296	71	91	13	13
14	VSS-M4S	UWF1, URF1	800	511	296	71	91	13	13
15	VSS-M2SM4S	UWF, URF1	813	511	296	71	91	13	13
16	QB - M3D	UWF0, URF0	813	392	296	71	91	13	13
17	QB - M4D	UWF1, URF1	813	444	296	71	91	13	13
18	QB_M3DM4D	URF, UWF0	803	75	296	70	87	13	13
19	QB_M1G	UWF1	793	375	296	71	91	13	13
20	QB_M2G	UWF0	813	362	296	71	91	13	13
21	QB_M1GM2G	UWF	803	239	296	71	91	13	13
22	M1G_M2G	UWF	793	239	296	71	91	13	13
23	M3G_M4G	NAF	257	498	296	71	91	13	13
24	BLB - M6S	URF	805	498	296	71	91	13	13
25	WL-M5GM6G	NAF	813	498	-	70	87	13	13

Table 7. Complete fault model dictionary for proposed open defect fault models with parasitic C values using 7 nm technology for 6T SRAM cell

S. No	Open defect between nodes	Fault model observed	Node Q C,fF	Node QB C in fF	Node WL C in fF	Node BL C in fF	Node BLB C in fF	Node VDD C in fF	Node VSS C in fF
	Fault free		1.7	1.5	0.77	0.62	0.81	0.31	0.31
1	BL-M5S	NAF	1.8	1.5	0.78	-	0.77	0.31	0.31
2	WL- M5G	NAF	1.8	1.5	0.6	0.6	0.82	0.31	0.31
3	WL- M6G	URF	1.8	1.5	0.52	0.63	0.82	0.31	0.31
4	Q-M1D	UWF1	1.4	1.5	0.78	0.63	0.82	0.31	0.31
5	Q-M2D	UWF0	1.5	1.5	0.78	0.63	0.82	0.31	0.31
6	Q-M1DM2D	NAF	0.68	1.5	0.73	0.63	0.82	0.31	0.31
7	Q-M3G	TF	1.6	1.5	0.78	0.63	0.82	0.31	0.31
8	Q- M4G	UWF1, URF1	1.6	1.5	0.78	0.63	0.82	0.31	0.31
9	Q-M3GM4G	NAF	1.3	1.5	0.78	0.63	0.82	0.31	0.31
10	VDD-M1S	UWF1	1.7	1.6	0.78	0.63	0.82	0.31	0.31
11	VDD-M3S	UWF0, URF0	1.8	1.6	0.78	0.63	0.82	0.31	0.31
12	VDD-M1SM3S	UWF, URF0	1.7	1.6	0.78	0.63	0.82	0.31	0.31
13	VSS-M2S	UWF0	1.7	1.6	0.78	0.63	0.82	0.31	0.31
14	VSS-M4S	UWF1, URF1	1.7	1.6	0.78	0.63	0.82	0.31	0.31
15	VSS-M2SM4S	UWF, URF1	1.8	1.6	0.78	0.63	0.82	0.31	0.31
16	QB - M3D	UWF0, URF0	1.8	1.2	0.78	0.63	0.82	0.31	0.31
17	QB - M4D	UWF1, URF1	1.8	1.3	0.78	0.63	0.82	0.31	0.31
18	QB_M3DM4D	URF, UWF0	1.7	0.7	0.78	0.6	0.77	0.31	0.31
19	QB_M1G	UWF1	1.6	1.5	0.78	0.63	0.82	0.31	0.31
20	QB_M2G	UWF0	1.8	1.4	0.78	0.63	0.82	0.31	0.31
21	QB_M1GM2G	UWF	1.7	1.3	0.78	0.63	0.82	0.31	0.31
22	M1G_M2G	UWF	1.6	1.3	0.78	0.63	0.82	0.31	0.31
23	M3G_M4G	NAF	1.3	1.5	0.78	0.63	0.82	0.31	0.31
24	BLB - M6S	URF	1.8	1.5	0.78	0.63	0.82	0.31	0.31
25	WL-M5GM6G	NAF	1.8	1.5	-	0.6	0.77	0.31	0.31

5. CONCLUSION

The intention of the work presented in this paper is to identify the effectiveness of open defects over short defect models in terms of parasitic resistance and capacitances observed at each node of faulty SRAM. Each defect model in terms of open and short are implied on single cell SRAM, that resulted with 21 open defect models in 32 nm technology and 25 open defect models in 7 nm technology. Out of these 46 fault

models, the unique fault models observed based on fault equivalence are TF, NAF, URF, USWF, USRF, SAF, UWF, IOF, WBAF, and USRF. Using the proposed method, we found existing fault models such as SAF, UWF, URF, TF, and NAF, along with an undetectable fault too such as UWARF. The proposed parasitic test method provides unbound fault coverage for static and dynamic faults including a few undetectable faults for single-cell SRAM. At the same time, the test method provides fault model dictionaries at the chosen technologies that helps in identification of fault syndrome with immediate analysis, also helps in yield improvement. As a future scope for this work, it can be extended for multiple cell SRAM architectures.

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AUTHOR CONTRIBUTIONS STATEMENT

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Parvathi Muddapu	✓	✓		✓	✓	✓		✓		✓		✓	✓	
Maddela Venkatesh	✓		✓			✓	✓	✓	✓		✓			

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors confirm that there are no conflicts of interest associated with this work.

DATA AVAILABILITY

Derived data supporting the findings of this study are available from the corresponding author [M. Parvathi] on request.

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