Bulletin of Electrical Engineering and Informatics
Vol. 13, No. 4, August 2024, pp. 2368~2380
ISSN: 2302-9285, DOI: 10.11591/eei.v13i4.7585

Ultra-low-power super class-AB adaptive biasing operational transconductance amplifier with enhanced gain for biomedical applications

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Article Info

Article history:

Received Sep 20, 2023
Revised Nov 19, 2023
Accepted Jan 15, 2024

Keywords:

Adaptive biasing
Adaptive load
Bulk-driven-flipped voltage follower
Low-power-operational transconductance amplifier
Low-voltage

ABSTRACT

The operational transconductance amplifier (OTA) proposed in this article is a bulk-driven (BD), single-stage, super-class-AB, adaptive biasing, functioning in the subthreshold region (ST) with an enormously low power supply of ± 0.25 V, providing high-gain. The input core of the OTA circuit is composed of adaptively biased BD differential input pairs based on flipped voltage follower (FVF), which drive in class-AB mode with a partial positive feedback (PPF) approach. The circuit additionally employs FVF and self-cascode (SC)-based low-power current mirror loads at its output to obtain significantly high gain and unity gain frequency. In addition, using adaptive loads based on source-degenerated metal oxide semiconductor (MOS) resistors raises dynamic current more efficiently, consequently improving the slew rate and unity gain frequency (UGF) without drawing additional power. Employing the cadence spectre tool and the UMC 0.18 µm complementary metal oxide semiconductor (CMOS) process technology, the designed OTA has been simulated. The simulation outcomes substantiate that the amplifier provides high open loop DC gain of 75 dB, 18.75 kHz UGF with a phase margin of 63.93º, and input-referred noise (IRN) of 0.734 µV/Hz$^{0.5}$ at 1 kHz frequency. The proposed OTA consumes just 60.15 nW of power. The performance results confirmed that the proposed OTA circuit is appropriate in biomedical applications.

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1. INTRODUCTION

The medical industry has undergone a significant shift towards portability in the last few years in consequence of the ongoing demand for battery-operated electronic devices, biomedical implantable devices, as well as energy-efficient portable biomedical gadgets, to routinely and continually monitor the patient's health. This is what draws attention to the creation of novel design methodologies for enormously low-voltage, low-power circuit designs that must be appropriate to the realm of biomedical applications [1]–[4]. For researchers, making analog and mixed-signal circuits in low-voltage conditions has created to be an insurmountable problem. This problem has become particularly considerable since complementary metal oxide semiconductor (CMOS) processes are continuously scaled down to increase device component density, so the supply voltage must also be proportionally reduced so as to maintain device consistency and minimize

power consumption. Scaling of supply voltage below 1V has become more challenging since metal–oxide–semiconductor field-effect transistor (MOSFET) threshold voltages and supply voltage scaling are not proportionally correlated [5]–[8]. Analog integrated circuits designers still continue to make significant contributions to this field and have provided several low-voltage design approaches, which are given in the literature [7]–[10].

Biomedical data acquisition systems operate towards the processing of the bioelectrical signals of the human body. Signals like electromyograms (EMGs), electrocardiograms (ECGs), electroencephalograms (EEGs), and other bioelectrical signals are low-frequency (just a few kHz) and low-voltage (amplitude range in μV to mV) signals [1], [3], [4]. In biomedical monitoring systems, the initial stage of signal processing is analog processing, which involves amplification and filtering. So, in the processing of biosignals, the front-end of the biomedical systems must have analog circuits that operate at low-voltage and utilize minimal power [3], [4]. The operational transconductance amplifier (OTA), the most fundamental building component is a key part of analog-front-end circuits in biomedical signal processing systems.

The fundamental requirements of the OTA exploited to amplify weak and noisy biosignals without loss are high and steady direct current (DC) gain, high common-mode rejection ratio (CMRR) (> 80 dB), high linearity, and rail-to-rail input/output swing with low noise and minimum power utilization (< 100 μW) [1]–[3], [7]. In lower technology nodes, it is quite difficult to achieve these features with a low power supply. In order to overcome threshold limitations, boost linearity, and decrease power consumption, the sub-threshold technique in amalgamation with the bulk-driven (BD) technique is advantaged more than the gate-driven technique for biomedical applications. The BD technique expands the rail-to-rail input/output range, however also increases input-referred noise (IRN), and reduces open-loop DC gain and unity gain frequency (UGF) since the ratio of bulk transconductance (g_{mb}) to gate transconductance (g_m) varies from 20% to 30% [11]–[13]. To address the aforementioned drawbacks of decreased bulk-transconductance in sub-1V conditions, lots of research has been done on bulk-transconductance, which is described in the literature [13]–[20] and also addressed in [21]–[23] under sub 0.5 V environments, used multi-stage BD-OTA to enhance DC gain. The performance of BD OTAs has been enhanced by exploiting current recycling technique [15], the positive feedback technique [14], [15], [21], [24] or positive position feedback (PPF) techniques [6], [10], [25]–[28], employ of an additional differential pair [18] in the input stage, or by using multi-stages OTA [13], [21], [22], [25], [29], [30]. Some authors use a self-cascode (SC) technique, as explained in literatures [6], [10], [14], [26] to carry a significant open loop voltage gain. All of the aforementioned techniques mostly enhance the small-signal responses of BD-OTAs by boosting open loop DC gain at the cost of either power, area or a sophisticated compensation circuit for improved stability.

This paper describes a BD super-class-AB sub-threshold OTA (BD-S-ST-OTA) that provides high-gain with minimal power consumption as well as low noise under ultra-low supply power. The proposed OTA circuit employs additional flipped voltage follower (FVF) and SC-based low-power current mirror loads at the amplifier's output in addition to adaptively biased BD-FVF differential input pairs operating in class-AB mode [10], [28], [31]–[33] in the input core with a partial positive feedback technique to attain considerably high gain and unity gain frequency. Additionally, using adaptive loads based on source-degenerated metal oxide semiconductor (MOS) resistors [31] results in more effective dynamic current boosting. Thus, by integrating the adaptive biasing technique with adaptive loads, the proposed BD-S-ST-OTA circuit enhances the dynamic current at the differential inputs and also at the active loads; hence, without drawing extra power, the UGF and slew rate are improved.

The following sections describe the structure of this paper. In section 2, the methods employed in the design of the proposed OTA, as well as its block-level simplified design and the circuit schematic, are illustrated. The complex design method analysis of the presented OTA in detail is covered in section 3. Section 4 covers the simulation outcomes of the presented circuit, along with process corner and Monte Carlo perusal. A comparison of the presented BD-S-ST-OTA with that of the other formerly published designs is also included in this section. The paper is eventually accomplished in section 5.

2. PROPOSED DESIGN METHOD

A block-level diagram and circuit schematic have been exploited to illustrate the methods employed in the creation of the proposed circuit design in order to accomplish the intended objectives of the work. The introduced high-performance BD-S-ST-OTA is represented in Figure 1 with a block-level simplified design that employs two similar BD FVFs and two identical BD P-MOS transistors M_{3a}, M_{3b} in the input core circuit. It works in the sub-threshold region. The FVF input pair is biased via a constant current source I_B, and the source terminals of transistors M_{3a}, M_{3b} are cross-connected to the output terminals Q and P of the FVF pair making the input core circuit adaptively biased, hence, the input pair functions in class-AB. The antiphase input signals of the bulk terminals of transistors M_{3a}, $M_{3b,}$ and the output terminals Q and P of the FVF input pair make the effective bulk transconductance of the input core circuit double. To once more raise

the transconductance, the PPF approach has been applied with transistors M_{7a} and M_{7b} at the active load ends of the input core, as illustrated in Figure 1. CM_1 and CM_2, source-degenerated MOS resistor-based nonlinear current mirrors having a current ratio of 1:1, are used as the active loads in the bottom side of the proposed OTA in order to boost the dynamic current and, consequently, the UGF. Along with all of these, two extremely effective FVF current mirrors (CM_3 and CM_4) and one SC current mirror CM_5 with a current transfer ratio of 1 are utilized as loads to transport input currents I_{O+} and I_{O-} originating by input transistor pairs M_{3a}, M_{3b} to the output and also increase the output impedance of BD-S-ST-OTA.

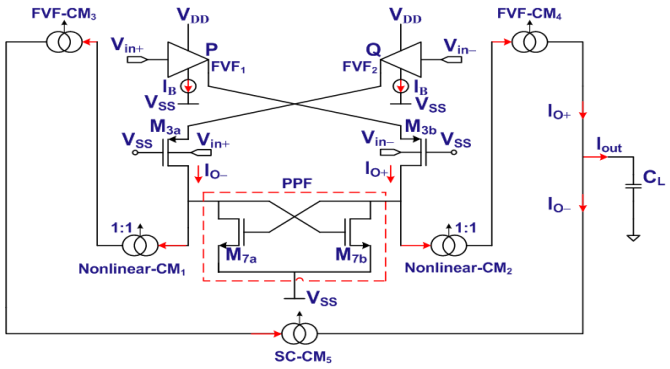

Figure 1. Simplified block-level schematic of the introduced BD-S-ST-OTA

The entire circuit schematic for the proposed BD-S-ST-OTA is exhibited in Figure 2. In the input stage, a BD-differential-pair is utilized to expand the input common-mode range (ICMR) of the circuit. However, a BD OTA's effective transconductance is much lower than that of a gate-driven OTA since the ratio of bulk transconductance (g_{mb}) to gate transconductance (g_m) varies from 20% to 30% [13]. As a result, the gain and UGF of the circuit also decrease significantly. To get over the above constraints, the input core of the BD-S-ST-OTA utilizes an adaptive biasing method and source degeneration MOS resistors-based adaptive loads that give extra dynamic current boosting, as detailed in [31].

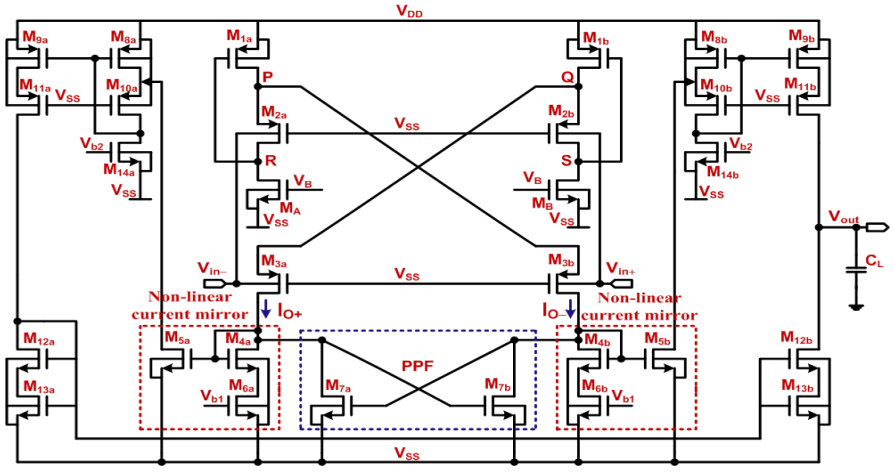

Figure 2. Proposed circuit schematic of BD-S-ST-OTA

The input core of the proposed OTA uses a similar pair of adaptively biased BD-FVF, made by BD P-MOSFETs M_{2a}–M_{2b}, diode-connected P-MOSFETs M_{1a}–M_{1b}, and the constant current source produced by N-MOSFETs M_A–M_B. The source terminal nodes P and Q of P-MOSFETs M_{2a}–M_{2b} have very low impedance due to the current shunt feedback offered by diode-connected P-MOSFETs M_{1a}–M_{1b}. Consequently, the proposed OTA's input core operates in class-AB, and the disadvantages of class-A circuits are significantly reduced by this process. Considering the FVF action, the two out-of-phase small input signals, when applied to the bulk terminals of the P-MOSFETs M_{2a}–M_{2b}, are transmitted to the output

terminals *P* and *Q*. The output terminals *P* and *Q* of the FVF pair are cross-connected to the source terminals of the adaptively biased differential pair M_{3a}–M_{3b}. The two antiphase small input signals are also applied to the bulk terminals of M_{3a}–M_{3b}; thus, the bulk terminals of M_{3a}–M_{3b} in combination with their source terminals, double the effective transconductance of the core circuit, which is equal to $2g_{mb2/3,a/b}$, since M_{2a}–M_{2b} and M_{3a}–M_{3b} have the same size. The differential input pair M_{3a}–M_{3b} and the adaptive loads ($M_{4a\text{-}6a}$ – $M_{4b\text{-}6b}$) make up the input core of the BD-S-ST-OTA. Adaptive loads ($M_{4a\text{-}6a}$ – $M_{4b\text{-}6b}$) used in the core circuit, are implemented using source degeneration MOS registers-based non-linear current mirrors [31], to offer more dynamic current boosting. The non-linear current mirrors employ a 1:1 current transfer ratio. Thus, by combining the adaptive biasing technique with adaptive loads, the proposed BD-S-ST-OTA circuit increases the dynamic current at the differential inputs and also at the active loads, thereby improving the slew rate and UGF.

The PPF technique described in [6], [10], [25]–[28] has been applied by exploiting transistors M_{7a} and M_{7b} at the adaptive load ends of the input core to move up the transconductance and gain further. Two highly efficient FVF current mirrors ($M_{8a\text{-}14a}$ – $M_{8b\text{-}14b}$) and one SC current mirror ($M_{12a\text{-}13a}$ – $M_{12b\text{-}13b}$) are employed to transmit the input currents I_{O+} and $I_{O-}$to the circuit's output and also raise the entire gain of the circuit by increasing the circuit's output impedance. In a SC structure, the two transistors are treated as a single composite transistor. To ensure that cascode transistors in SC current mirrors are saturated in weak-inversion, their aspect ratios are multiplied by 20 in comparison to the comparable transistors connected to the supply side. The output impedance typically rises by a factor of 10, comparable to a gain increase of approximately 20 dB, when SC loads are utilized [6], [10], [14], [26], [33]. Thus, the overall performance of the proposed BD-S-ST-OTA has significantly increased.

3. CIRCUIT DESIGN METHOD ANALYSIS

In order to analyze the circuit design method of the proposed BD-S-ST-OTA, we have to study its small signal analysis, stability analysis, and noise, which are all discussed in this section.

3.1. Small signal analysis

The effective overall transconductance, voltage gain, and UGF of the proposed BD-S-ST-OTA are all analyzed under this analysis.

3.1.1. Effective overall transconductance

The input core circuit of the proposed BD-S-ST-OTA is indicated in Figure 3(a), and for calculating its overall effective transconductance, its half-circuit corresponding small signal model is revealed in Figure 3(b). The proposed circuit is symmetrical; similar transistors have been used on both sides of the circuit. The bulk terminals of transistors $M_{2,3,a}$ and $M_{2,3,b}$ be given the input signals $-V_{id}/2$ and $V_{id}/2$, respectively. The source potentials of transistors M_{2a} and M_{3b} are represented as V_P, while the gate potential of transistor M_{1a} and the drain potential of transistor M_{2a} are both represented as V_R. A constant current source I_B produced by transistors M_A and M_B, is used to produce the biasing current for input transistor pairs M_{2a} and M_{2b}. Consider the small signal model exposed in Figure 3(b), the small signal current flowing via transistor M_{2a} at node *R* is zero [31], and is expressed as (1):

$$(V_P - V_R)g_{ds2,a} - g_{mb2,a}\left(-\frac{V_{id}}{2} - V_P\right) - g_{m2,a}(-V_P) = 0 \quad (1)$$

Neglecting the term $g_{ds2,a}$ since its value is much lower than the others hence (1) can be rewritten as (2) and (3):

$$g_{mb2,a}\left(\frac{V_{id}}{2} + V_P\right) + g_{m2,a}(V_P) = 0 \quad (2)$$

$$V_P = \frac{-g_{mb2,a}{}^{V_{id}}/_2}{(g_{m2,a}+g_{mb2,a})} \quad (3)$$

The output small signal current I_{O-} contributed by transistor M_{3b}, is sourced by transistor M_{1a} [31], and is written as (4):

$$I_{O-} = -g_{m3,b}(-V_P) - g_{mb3,b}\left(\frac{V_{id}}{2} - V_P\right) + \left(V_P - V_{D3,b}\right)g_{ds3,b} \quad (4)$$

Neglecting the term $g_{ds3,b}$, then (4) can be rewritten as (5):

$$I_{O-} = \left(g_{m3,b} + g_{mb3,b}\right)V_P - g_{mb3,b}\frac{V_{id}}{2} \quad (5)$$

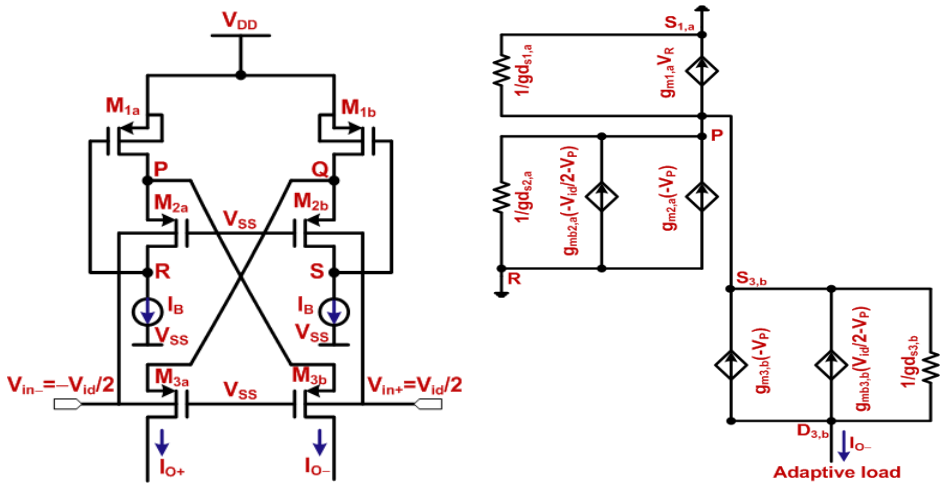

Figure 3. Circuit: (a) core circuit for the BD-S-ST-OTA and (b) half sub-circuit equivalent small signal model

Using the value of V_P from (3), then (5) results as (6):

$$I_{O-} = -\left(g_{m3,b} + g_{mb3,b}\right)\frac{g_{mb2,a}{}^{V_{id}}/_{2}}{(g_{m2,a}+g_{mb2,a})} - g_{mb3,b}\frac{V_{id}}{2} \quad (6)$$

As a result of the similarity of the transistors on the two sides of the input core circuit, $g_{m2,a}$=$g_{m3,b}$ and $g_{mb2,a}$=$g_{mb3,b}$. By including these relationships in (6), the value of I_{O-} can be expressed more simply as (7):

$$I_{O-} = -2g_{mb3,b}\frac{V_{id}}{2} \quad (7)$$

Similarly, the expression for output current I_{O+} of the input core is given as (8):

$$I_{O+} = 2g_{mb3,a}\frac{V_{id}}{2} \quad (8)$$

The input core transconductance is basically defined as (9):

$$G_{m,input\ core} = \frac{(I_{O+}-I_{O-})}{(V_{in+}-V_{in-})} \quad (9)$$

Thus, using (9), the proposed amplifier's input core transconductance is expressed as (10):

$$G_{m,input\ core} = 2g_{mb3} \quad (10)$$

Taking into account the influence of the PPF loop employing by the transistors M_{7a}–M_{7b} and the current gain K_1=1 of source degenerated MOS resistor-based nonlinear current mirrors, the BD-S-ST-OTA's total effective transconductance is calculated as (11):

$$G_{m,effective}|_{BD-S-ST-OTA} = K_1\frac{2g_{mb3}}{(1-\alpha)} = \frac{2g_{mb3}}{(1-\alpha)} \quad (11)$$

where K_1 is the current gain and α is the transistor's aspect ratio and are given as $K_1 = \frac{g_{m5}}{g_{m4}} = 1$ and $\alpha = \frac{g_{m7}}{g_{m4}}$. To prevent stability issues with a shift in the location of the pole, it is preferable that the value of α be set to $0 < \alpha < 1$.

3.1.2. Voltage gain

For the proposed BD-S-ST-OTA, the open loop voltage gain is typically calculated by the multiplication of the circuit's effective transconductance and output impedance. The circuit has a SC load

and an FVF current mirror load parallel at the output node; hence the complete circuit's output impedance is expressed as (12):

$$R_{out} = \left(g_{m11,b}g_{ds11,b}g_{ds9,b}\right)||\left(g_{m12,b}g_{ds12,b}g_{ds13,b}\right) \quad (12)$$

Thus, the overall voltage gain of the BD-S-ST-OTA, as defined is provided by (13):

$$A_V|_{BD-S-ST-OTA} = G_{m,effective}|_{BD-S-ST-OTA} \cdot R_{out} = \frac{2g_{mb3}}{(1-\alpha)}\left(g_{m11,b}g_{ds11,b}g_{ds9,b}\right)||\left(g_{m12,b}g_{ds12,b}g_{ds13,b}\right) \quad (13)$$

The UGF of the proposed BD-S-ST-OTA is expressed as (14):

$$\frac{G_{m,effective}|_{BD-S-ST-OTA}}{2\pi C_L} = \frac{1}{2\pi C_L}\frac{2g_{mb3}}{(1-\alpha)} \quad (14)$$

The proposed OTA's improved effective transconductance value leads to a larger UGF.

3.2. Stability analysis

Without the use of a compensating capacitor, the proposed BD-S-ST-OTA maintains steady operation with high DC gain. Owing to output impedance and capacitive load, the BD-S-ST-OTA provides a dominant pole (p_1) at the output node. This is stated as (15):

$$p_1 = \frac{1}{R_{out} \cdot C_L} \quad (15)$$

3.3. Noise analysis

The OTA must have the least amount of input-referred output noise for biological applications. The thermal and flicker noises are two of the main noise sources that the MOS transistor itself produces. A MOS transistor's maximum noise current spectral density as described in the literature [10], [11], is provided by (16):

$$\overline{i_o^2} = \overline{i_{o,th}^2} + \overline{i_{o,(1/f)}^2} = \left[4k_BT\gamma g_{mi} + \frac{K_f g_{mi}^2}{(WL)_i C_{ox} f}\right] \cdot \Delta f \quad (16)$$

where T is the absolute temperature, k_B is boltzmann's constant, γ is ½ for sub-threshold operated devices, g_{mi} is the concerned MOS transistor's gate transconductance, K_f is the flicker noise constant, and is process-dependent, W and L are the concerned MOS transistor's width and length, and f is the frequency, respectively.

Using the procedures described in the reference [10]–[12], the expression for bulk-input referred thermal noise per unit bandwidth of the BD-S-ST-OTA including FVF, non-linear current mirror load, PPF, and FVF current mirror as well as SC current mirror loads is provided by (17):

$$\overline{V_{in,B,th}^2} = \frac{4k_BT}{G_{m,effective}^2|_{proposed}}\left[g_{m1} + g_{m2} + g_M + g_{m3} + \left(1 + \frac{g_{m7}}{g_{m4}}\right) \cdot g_{m4} + g_{m5} + g_{m8} + g_{m9} + g_{m13} + g_{m14}\right]\Delta f \quad (17)$$

Similarly, under the assumption that all transistors positive MOS (NMOS) or negative MOS (PMOS) of similar type in the proposed OTA have the same K_f, the expression for flicker noise per unit bandwidth for the BD-S-ST-OTA including FVF, non-linear current mirror load, PPF, and FVF current mirror as well as SC current mirror loads is provided by (18):

$$\overline{V_{in,B,(1/f)}^2} = \frac{2}{G_{m,effective}^2|_{proposed}}\left[\left\{\frac{g_{m1}^2}{(WL)_{1a,b}} + \frac{g_{m2}^2}{(WL)_{2a,b}} + \frac{g_{m3}^2}{(WL)_{3a,b}} + \frac{g_{m8}^2}{(WL)_{8a,b}} + \frac{g_{m9}^2}{(WL)_{9a,b}}\right\}\frac{k_{fp}}{C_{ox} \cdot f} + \left\{\frac{g_M^2}{(WL)_{MA,B}} + \left(1 + \frac{g_{m7}}{g_{m4}}\right) \cdot \frac{g_{m4}^2}{(WL)_{4a,b}} + \frac{g_{m5}^2}{(WL)_{5a,b}} + \frac{g_{m13}^2}{(WL)_{13a,b}} + \frac{g_{m14}^2}{(WL)_{14a,b}}\right\}\frac{k_{fn}}{C_{ox} \cdot f}\right]\Delta f \quad (18)$$

IRN for biological signal processing or at low frequencies is primarily made up of flicker noise, and it can be diminished by increasing overall $G_{m,effective}$ of the proposed BD-S-ST-OTA and size of each MOSFETS, especially N-MOSFETS since N-MOSFET contributes more flicker noise.

4. RESULTS AND DISCUSSION

4.1. Simulation results

To exhibit the higher performance achieved by the circuit design shown in Figure 2, the designed OTA is simulated with a dual supply power of ± 0.25 V for a 15 pF load capacitor. The simulation has been performed at a reference temperature of 27 °C by utilizing the UMC 180 nm standard CMOS technology on the cadence virtuoso system design simulator. The constant current I_B to bias the BD-FVF input pair in BD-S-ST-OTA is produced by N-MOSFETs M_A–M_B and is set to 18 nA. Operating in the weak-inversion region for utilization of nominal power, the BD-S-ST-OTA has a total stand-by current of 120.3 nA. The FVF current mirror employed at the circuit's output is biased by the 1.2 nA constant current source produced by the N-MOSFETs $M_{14a/b}$. The gate of the source degeneration transistors (M_{6a}–M_{6b}) in the adaptive loads ($M_{4a\text{-}6a}$–$M_{4b\text{-}6b}$) is biased by a voltage V_{b1} in the ohmic region but close to the saturation region's edge. When subjected to high input currents, degeneration transistors (M_{6a}–M_{6b}) enter the saturation region. Thus, a significantly nonlinear equivalent resistance is obtained, leading to a significant increase in output current. Additionally, to mitigate the effects of IRN and channel length modulation in the circuit, each MOSFET in the design also has an optimized aspect ratio.

One of an OTA's most important performance factors is noise. Due to supply variations or component mismatches, it often couples to the desired signal, creating an undesirable output. Flicker noise is more prevalent in biomedical applications since bio signals have a frequency range of 10 mHz ≤ *fbio* ≤ 1 kHz. So, for biomedical applications, the OTA should assure the least amount of IRN at output. Owing to the low flicker noise offered by PMOS devices, PMOS devices have been utilized in the proposed amplifier in the input-pair. The IRN value for the BD-S-ST-OTA, which is 0.734 μV/Hz$^{0.5}$ at 1 kHz, is exposed in Figure 4. Its value is less because of the improved overall input core transconductance of the circuit.

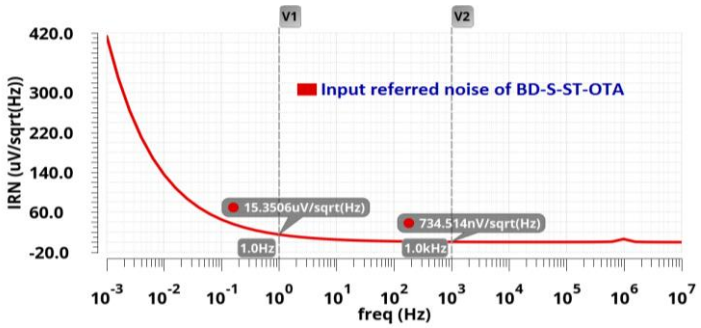

Figure 4. Plot of the IRN of the BD-S-ST-OTA

The proposed BD-S-ST-OTA's open-loop AC plot is depicted in Figure 5, and the simulation results reveal that it maintains a stable operation with a PM of 63.93° and provides an open-loop DC gain of 75 dB and a UGF of 18.758 kHz while using only 60.15 nW of power. Furthermore, Figure 6 illustrates that at 1 mHz, this OTA offers a high power supply rejection ratio (PSRR) (+/–) and CMRR, with values of 94.74 dB/93.96 dB, and 158.02 dB, respectively.

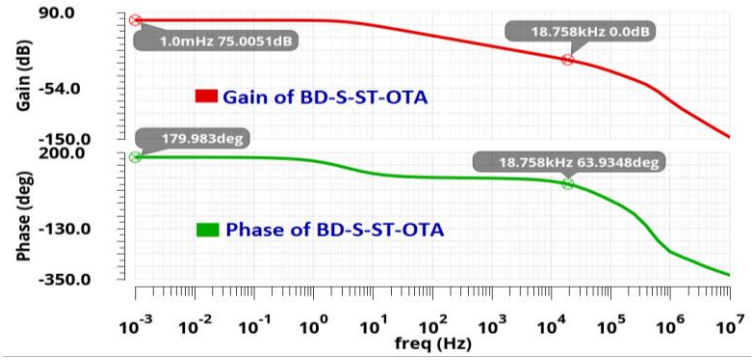

Figure 5. Plot of the BD-S-ST-OTA's AC response

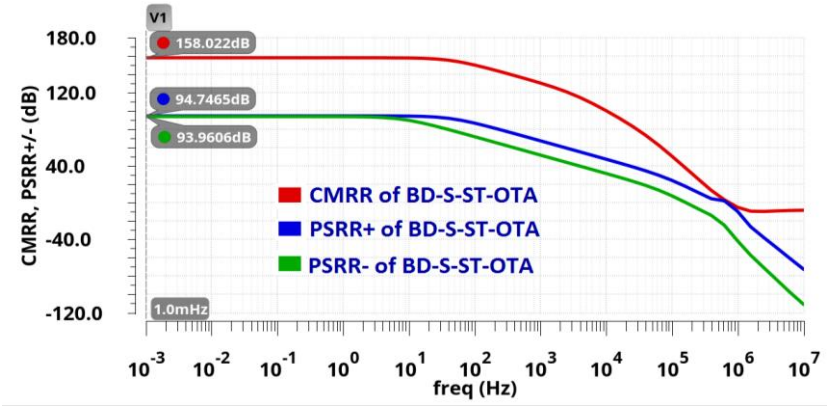

Figure 6. Plot for the proposed BD-S-ST-OTA's (PSRR+/–) and CMRR

To accomplish the transient response of large signals, Figure 7 depicts a voltage follower design of the BD-S-ST-OTA by coupling its inverting input to output. The voltage follower's output response is depicted in Figure 8 for a 15 pF load capacitor after applying a square wave with ± 0.25 V amplitude and 400 Hz frequency as an input signal to the non-inverting input terminal. The calculated SR_{av} for the BD-S-ST-OTA is 1.784 V/ms.

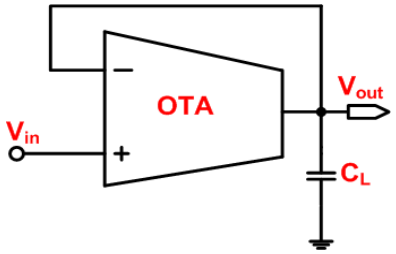

Figure 7. BD-S-ST-OTA as a voltage follower structure

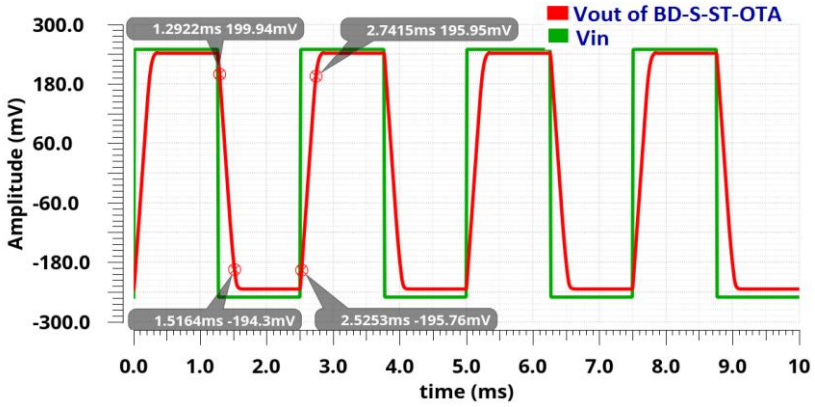

Figure 8. Large-signal pulse response of BD-S-ST-OTA to $V_{in,peak}$=±0.25 V at 400 Hz square wave

To assess the sinusoidal transient response, apply a sinusoidal input signal with a $V_{in,peak}$ of 250 mV and a common-mode voltage (V_{cm}) of 0V to the non-inverting input terminal in Figure 7. The output of the simulation is displayed in Figure 9, which demonstrates that the proposed BD-S-ST-OTA delivers an output signal swing of (-233.54 mV–242.29 mV). The output voltage swing is just about rail-to-rail (95.16%) with an offset voltage of no more than 16.46 mV.

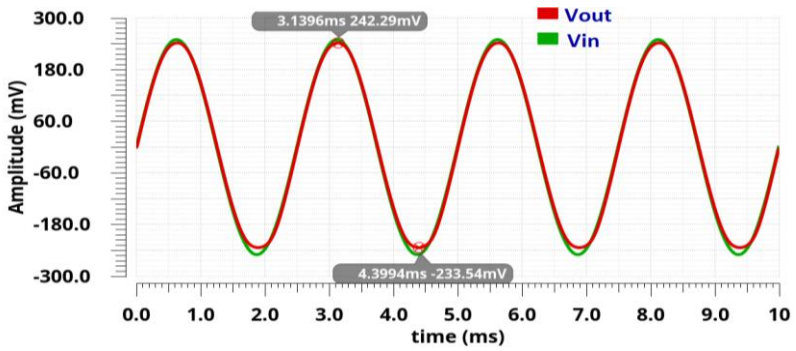

Figure 9. Transient response of a sinusoidal signal for V_{cm}=0V and $V_{in,peak}$=250 mV

To determine the ICMR, a DC transfer analysis of the BD-S-ST-OTA in a voltage follower configuration with a capacitive load of 15 pF is assessed. The simulation's outcome is revealed in Figure 10. The proposed BD-S-ST-OTA exhibits linearity over a wider range of ICMR with a small offset voltage variation across the entire input voltage range.

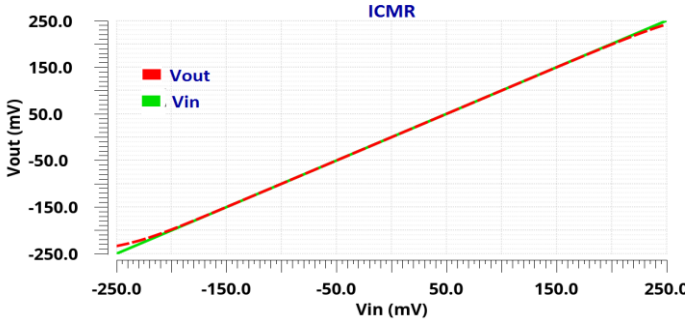

Figure 10. ICMR of BD-S-ST-OTA in voltage follower configuration as a result of DC sweep

The BD-S-ST-OTA's total harmonic distortion (THD) is examined to evaluate its linearity over the entire signal's swing range. A sinusoidal signal with a peak amplitude ranges from 25 mV to 250 mV and a frequency of 400 Hz is input to the voltage follower arrangement of the BD-S-ST-OTA, and the simulation outcome is depicted in Figure 11. At 100 mV of peak amplitude, the THD of the input sine wave for the BD-S-ST-OTA is-50.27 dB, and up to 210 mV of peak amplitude, it is beneath 1%. For sine wave amplitudes between 25 mV to 250 mV, the THD range is from-62.99 dB to-32.82 dB. Thus, it offers the THD of only-32.82 dB (2.28%) in the case of rail-to-rail signal swings of input and output.

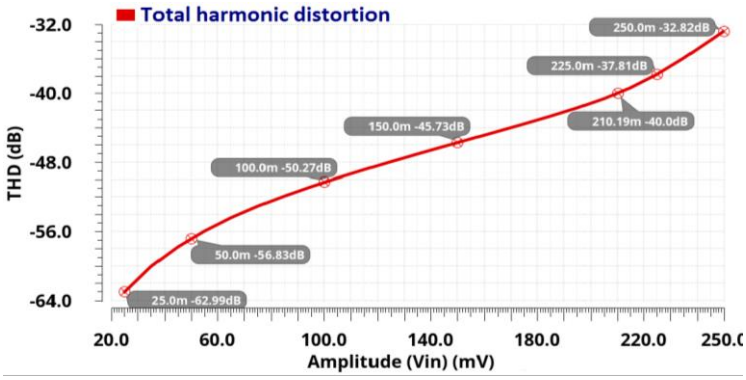

Figure 11. THD variation against peak amplitude at 400 Hz frequency for BD-S-ST-OTA

The performance parameters deviation from the process and mismatch are used to gauge the OTA's robustness. Utilizing Monte-Carlo sampling with 200 samples, the robustness of OTA's parameters has been studied, and the results of OTA's parameters, including IRN, DC gain, preventive maintenance (PM), and UGF, are displayed in Figure 12 in histogram form. The outcomes shown in Figures 12(a) to (d) indicate low standard deviations (SD) for all of the parameters; hence, the proposed BD-S-ST-OTA is insensitive to process variation. Table 1 provides a detail of the performance parameters results from the Monte-Carlo simulation.

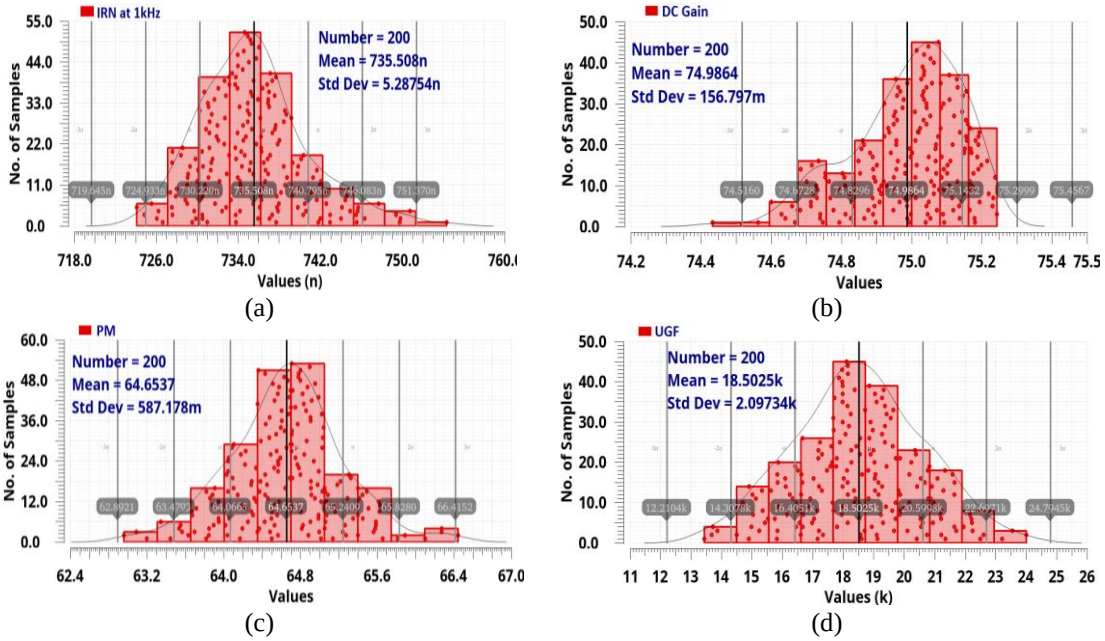

Figure 12. Outcomes of a Monte Carlo iteration using 200 samples of: (a) IRN, (b) DC gain, (c) PM, and (d) UGF

Table 1. Outcomes for 200 samples of Monte Carlo sampling of the proposed BD-S-ST-OTA

Parameters	Mean (μ)	SD (σ)
IRN (nV/Hz$^{0.5}$) at 1 kHz	735.508	5.287 n
Total current (nA)	119.3	13.07 n
Open loop DC gain (dB)	74.986	156.797 m
Phase margin (degree)	64.65	587.178 m
UGF (kHz)	18.502	2.097
CMRR (dB) @1 mHz	150.1	9.995
PSRR+ (dB) @1 mHz	94.73	803.1 m
PSRR–(dB) @1 mHz	93.93	667.1 m
SR(av) (V/ms)	1.803	125.4 m
Total power (nW)	59.673	6.537 n

Due to defects in the manufacturing process, integrated circuits (IC) fabrication is considerably impacted, especially at lower technology. Additionally, the circuit should be able to function adequately in conditions of mild temperature variation and modest supply voltage fluctuation. Corner analysis for five different corners (TT, SS, FF, SNFP, and FNSP) at 27°C has been performed to assess how sensitive the proposed BD-S-ST-OTA is to variations in the process. The performance of the BD-S-ST-OTA has also been confirmed by altering the supply voltage by ±10% and the temperature from –5 °C to +60 °C. Table 2 contains a summary of the simulation results for the performance parameters in relation to PVT (process, voltage, and temperature) fluctuations. The condensed results exhibit that, with only a little variation in the UGF, the BD-S-ST-OTA consistently maintains its performance under fluctuations in PVT conditions.

4.2. Comparisons and discussion

The performance effectiveness of OTA in terms of small-and large-signals as stated in [23], [24] is provided in (19) and (20) with the help of two significant figures of merit (FOM_{Sm}, FOM_{La}). FOM_{Sm} and FOM_{La} represent the small and large signal responses, respectively. Table 3 provides a summary of the BD-S-ST-OTA's performance attributes.

Table 2. PVT fluctuations and the performance of the BD-S-ST-OTA

Parameters	Corner evaluation at 27°C					(V_{DD} + $\|V_{SS}\|$) ±10% Variation of supply		Variation of temperature	
	TT	SS	FF	SNFP	FNSP	0.45 V	0.55 V	−5 °C	+60 °C
IRN (nV/Hz$^{0.5}$) at 1 kHz	734.5	826.3	707.6	735.8	735.9	813.902	700.339	708.5	795.9
Open loop DC gain (dB)	75.005	75.077	74.611	73.0893	71.242	69.88	78.77	76.199	71.69
UGF (kHz)	18.758	6.427	49.46	9.422	20.403	6.915	48.25	6.258	38.88
Phase margin (degree)	64.6	68.66	57.54	74.61	67.24	70.22	53.79	68.696	58.3

Table 3. Summarized performance parameters of BD-S-ST-OTA

Parameters	BD-S-ST-OTA
Technology	0.18 µm
Total current (nA)	120.3
Open loop DC gain (dB)	75.005
Total power (nW)	60.15
Load capacitance (pF)	15
IRN (µV/Hz$^{0.5}$) at 1 kHz	0.734
CMRR (dB) @1 mHz	158.02
Phase margin (degree)	63.935
PSRR+(dB) @1 mHz	94.743
UGF (kHz)	18.758
Power supply (V)	± 0.25
PSRR−(dB) @1 mHz	93.96
$SR_{(av)}$ (V/ms)	1.784
FOM_{Sm}	2.34
FOM_{La}	0.222

Table 4 compares the proposed BD-S-ST-OTA's performance characteristics with some of the other recent OTAs. The proposed BD-S-ST-OTA has the utmost DC gain, PSRR (average) compared to the others, with minimal power consumption. In addition, with the exception of [15] only, it has a maximum CMRR. Under the limitations of low-voltage of sub-1V, the proposed BD-S-ST-OTA has offered the second-highest small-signal response (FOM_{Sm}), while it does not provide the maximum large-signal response FOM_{La}. Compared to other OTAs, except for [21], the small-signal response FOM_{Sm} is around twice as high. The proposed OTA's competence is confirmed by computed parameters given in Table 4.

$$FOM_{Sm} = \frac{UGF(MHz)\times C_L(pF)}{I_T(\mu A)} \quad (19)$$

$$FOM_{La} = \frac{SR_{av}(V/\mu s)\times C_L(pF)}{I_T(\mu A)} \quad (20)$$

Table 4. Comparison of the BD-S-ST-OTA's performance to formerly OTA designs at 0.18 µm technology

Parameters	This-work 2023	[14] 2017	[17] 2017	[18] 2018	[22] 2018	[15] 2019	[20] 2020	[27] 2021	[30] 2023	[21] 2022
IRN[a] @ (µV/HZ$^{0.5}$)	0.734	2.53	6.25 @ 0.1Hz	–	1.85[S]	0.25@ 0.1Hz	0.173	0.779	53.7	–
Total current (nA)	120.3	125	275	62,000	51	240	6,500	200	104,000	60
Input drive	BD	BD	BD	BD	BD	BD	BD	BD	DTMOS	BD
PM (º)	63.935	54	62.45	87	61.2	74	57.5	89.07	72.16	60
Total power (nW)	60.15	64	165	49,600	15.3	144	2600	140	104,000	24
Results	S	S	S	S	E	S	S	S	S	E
(DC gain)[b] (dB)	75.005	70.4	61.5	44.3	65.8	71@ 0.1Hz	72.6	71.35	73.86	60
Supply voltage (V)	±0.25	0.5	0.6	0.8	0.3	0.6	0.4	0.7	± 0.5	0.4
UGF (MHz)	0.01875	0.009	0.03015	1.45	0.0028	0.0182	0.322	0.00107	15.36	0.007
CMRR[b] (dB)	158.02	106	–	–	72	201.8@ 10Hz	110.8	138.5	121.87	85
PSRR[b]+(dB)	94.743	70	67.9	–	62	77.4@ 10Hz	103	77.08	–	76
PSRR[b]−(dB)	93.96	–	–	–	–	–	–	60.23	–	–
C_L(pF)	15	15	12	50	20	15	5	50	10	30
SR_{av} (V/µs)	0.00178	0.967	0.0553	3.5	0.0071	0.0066	0.214	0.00157	168	0.079
FOM_{Sm}	2.34	1.11	1.31	1.17	0.784	1.13	0.25	0.27	1.48	3.5
FOM_{La}	0.222	116.0	3.01	2.82	2.54	0.412	0.164	0.39	16.15	39.5

* a: at 1 kHz, b: at 1mHz, av: average, E: experimental, S: simulation

5. CONCLUSION

The work in this article describes a low-voltage, enhanced-gain, and power-effective BD-single-stage super-class-AB OTA that utilizes dual supply power of ± 0.25 V and functions in the sub-threshold region. The proposed BD-S-ST-OTA circuit attains extensively large gain, dynamic current, and unity gain frequency by employing highly-effective current mirrors based on SC and FVF at the amplifier's output in addition to adaptively biased BD-FVF differential input pairs driving in the class-AB mode in the input core together with PPF approach. Additionally, utilizing source degenerated MOS resistor-based adaptive loads offers greater dynamic current. The simulation outcomes demonstrate that the proposed circuit offers a maximum DC gain of 75 dB, a UGF of 18.75 kHz, and a phase margin of 63.935, with just 60.15 nW of power consumption. Its IRN is only 0.734 μV/√Hz at 1 kHz frequency. Up to 210 mV of peak amplitude, the THD of the input sine wave for the BD-S-ST-OTA in its voltage follower configuration is less than 1%. The obtained results from the amplifier listed in Table 3 confirmed that the proposed BD-S-ST-OTA is suitable for low-frequency sensors, used as an analog front-end circuit for amplifying biomedical signals in biomedical systems, and low-voltage applications.

ACKNOWLEDGEMENTS

We express our gratitude to the journal team for providing valuable suggestions to prepare this manuscript in well form.

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